

Power Architecture™ '07
DEVELOPER CONFERENCE



MPC5121e: Automotive-Qualified Multi-Core Microprocessor for Telematics and Beyond

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Power.ORG ™

The Telematics Challenge



- » Connected Experience
 - Audio/visual entertainment
 - Voice and data connectivity
 - Real-time navigation and information services
- » Safe Environment
 - Hands-Free voice activated HMI with inference
 - Emergency recognition and response processing
 - Accident avoidance through vision/RADAR
- » Technical Challenges
 - Vibration and mechanical stresses
 - Wide temperature operating range
 - Dynamically changing contextual operating environment
 - Low-cost products with a long lifetime and production cycle

The telematics market provides a **unique challenge** to reproduce the home/office/mobile/vehicle connected experience, augmented with a **safe** and autonomous nature, in a **robust long-life** product that must overcome **difficult technical challenges**.

Automotive Versus Consumer Requirements



» Cost

- Automotive: Heavy integration, larger ball pitch to reduce board complexity
- Consumer: Heavy integration, small package body to reduce board size

» Power/leakage

- Automotive: Minimize for packaging cost and extended key off battery life
- Consumer: Minimize for operating battery life

» Product development and lifetime

- Automotive: 2 years dev, 10 years life
- Consumer: 10 month development, 2 years life

» Environmental conditions

- Automotive: -40 to 85/100°C ambient
- Consumer: 0 to 70°C ambient

» Design methodology

- Automotive: 0 PPM (zero defect), AEC-Q100, TS14969
- Consumer: High PPM acceptable

» Design for automotive, leverage for other applications

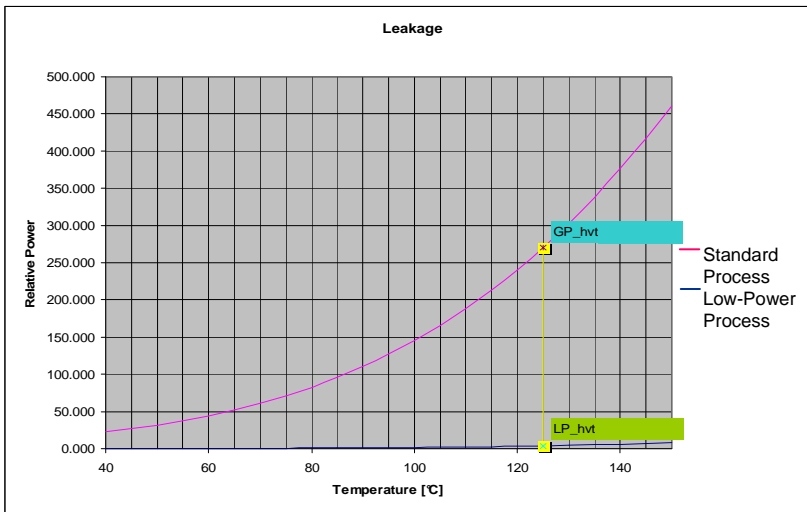
- Integration focused on flexibility and better long-range projections
- Strong focus on zero defect development and production cost reductions
- Repackage for potential applications that require minimal board footprint

Development Paradigm Shift



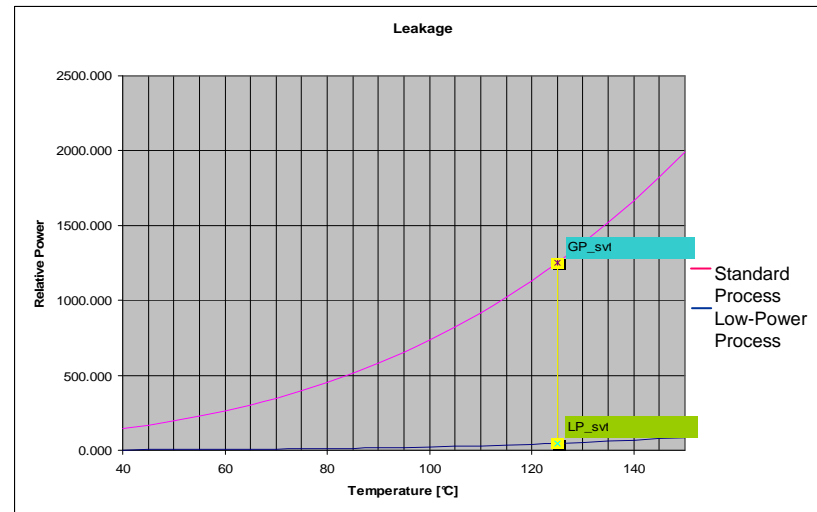
- » Why a low-power device technology?
 - High temperature has a dramatic effect on leakage
 - Leakage reduction enables higher device integration levels
 - Leakage reduction affects transistor performance
- » What about the application performance requirements?
 - Increase performance with supply voltage levels -> more dynamic power
 - However 85% dynamic of total power consumption under application control!
 - Voltage/frequency chosen to optimize a given application
 - Static and dynamic clock gating to avoid unnecessary activity
 - Low power sleep modes to capitalize on application inactivity
 - Sub-50uA deep sleep leakage mode with RTC, CAN and GPIO wakeup
 - Integrated temperature sensor to monitor junction temperature
 - Employ power/performance efficient multi-core architecture
 - General CPU processing power is by nature not as efficient as specialized cores
 - Operate more parallelism at lower frequencies to achieve a given performance level

Low-Power Technology Selection



Low Leakage Devices (high Vt)

- 114X LP->GP @85C
- 70X LP->GP @125C
- 4.0X 50C-> 85C in LP
- 4.6X 85C->125C in LP

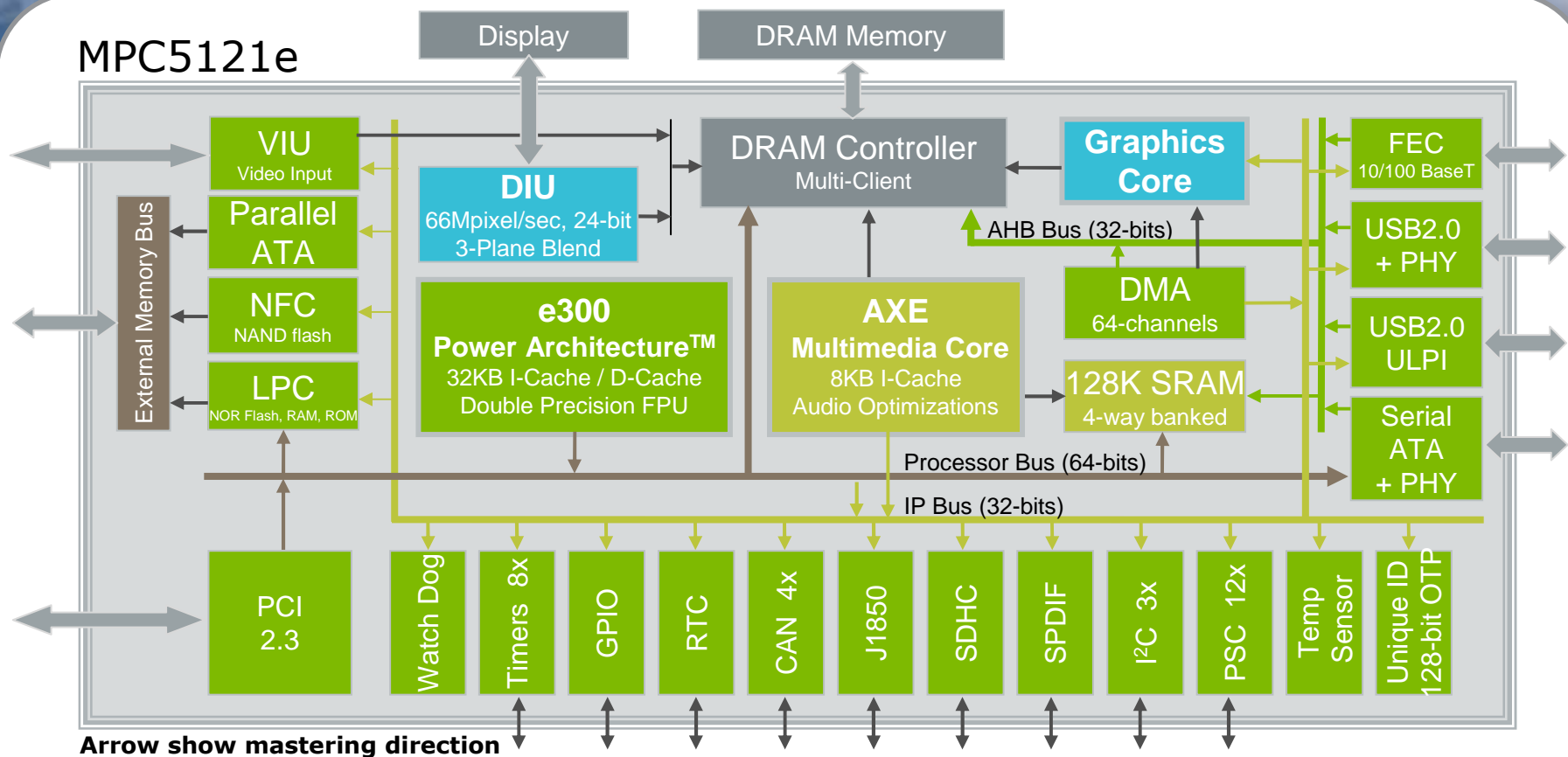


Performance Devices (standard Vt)

- 37X more leakage @85C
- 27X more leakage @125C
- 3.5X 50C-> 85C in LP
- 6.2X 85C->125C in LP

- » High temperature has a dramatic affect on leakage
- » Leakage is statically driven by integration rather than operating conditions
- » Beware of how power consumption and leakage is specified!

MPC5121e SoC Architecture



- ▶ Multi-core architecture improves the power/performance trade-off through more efficient computing
- ▶ Multi-client DRAM controller architecture achieves a simulated throughput of 1100Mbytes/sec
- ▶ Peripheral integration which absorbs system BOM cost across many applications

Heterogeneous Multi-Core Advantages



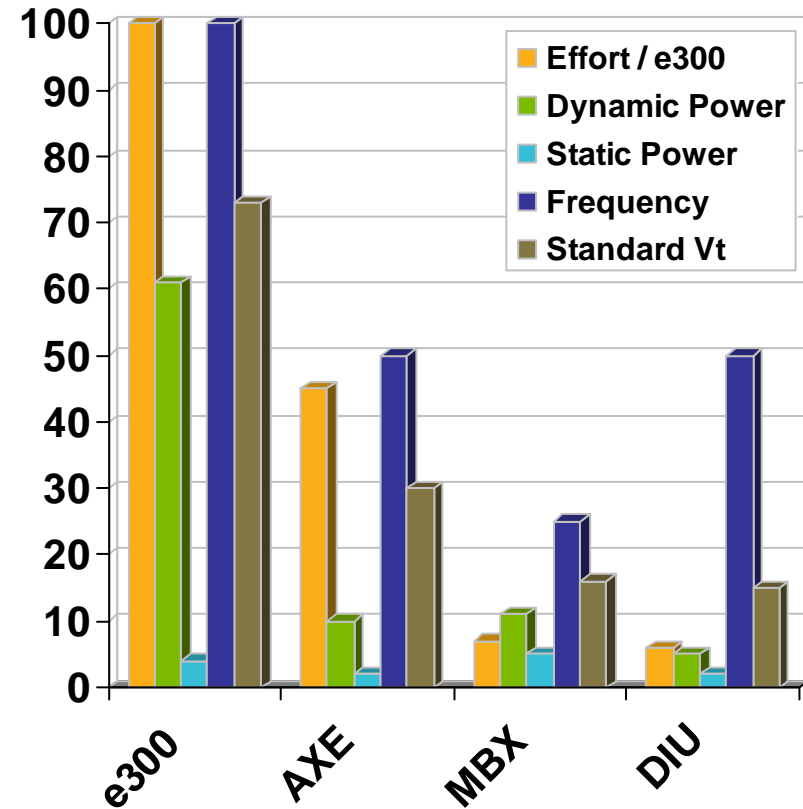
» Application specific cores improve efficiency of computation

- Effort shows the accelerator load as compared to e300 load to run a given application normally addressed by the accelerator targeted at that application.
- Dynamic & static shown as percentages of sum total power of all accelerators
- Frequency shown percentage of e300 frequency
- Standard Vt shows percentage of high performance transistors

Multimedia Acceleration Core (AXE): End-user programmable core using a complete C language development environment

MBX: 2D/3D graphics accelerator core (end user programmable core using OpenGL/OpenVG standards)

DIU: Graphics bending and display interface unit (non-programmable parameterized block)



Power Architecture™ Continuum



» Leverage MPC5200 market penetration

- MPC5121e is 100% binary compatible with MPC5200
- Maintain same feature set at or above the MPC5200 level of performance

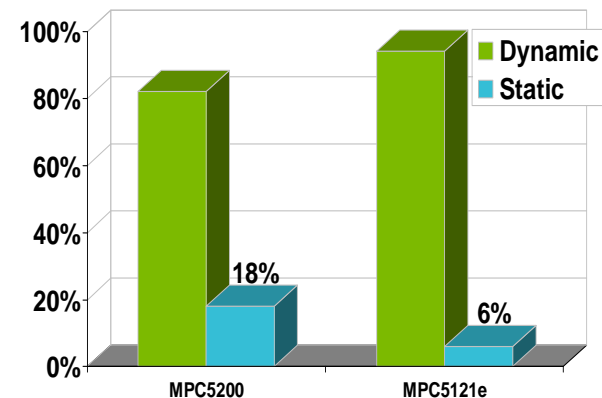
» e300 Features

- 4-stage dual-issue out-of-order pipeline (up to 3 issued/retired, 5 executing)
- Programmable static branch prediction (compiler) with branch folding
- 32x 32-bit general purpose and 32x 64-bit floating point register files
- IEEE 754-compliant double precision floating point
- Full hardware support for little endian applications

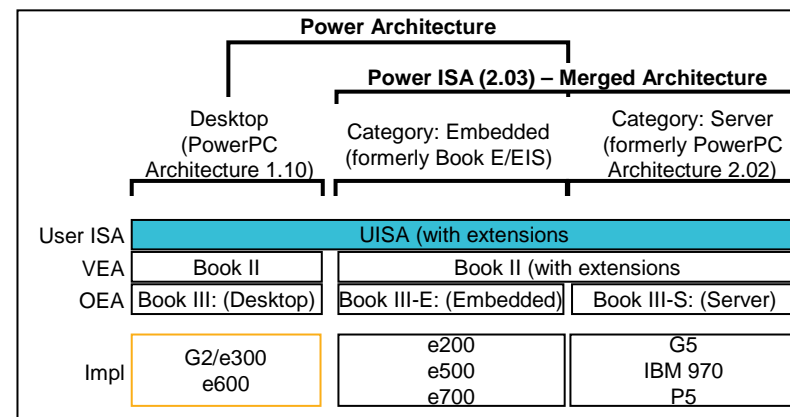
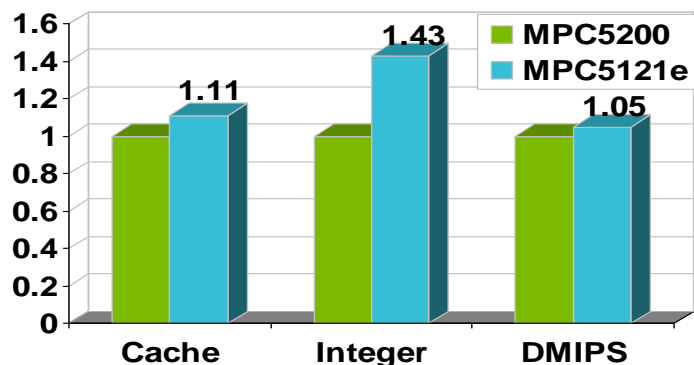
» MPC5121e enhancements over MPC5200

- First e300 low-leakage device technology port
- Instruction/data cache doubled to 8-way 32K
- Reduced integer multiply to 2-cycles from 6-cycles, added 2nd integer ALU
- **4.6X** dual multiply-accumulate speedup (13/7-cycs -> 3/1.5-cycs latency/throughput)
- Added BIU capability to enable multi-e300 L2 cache subsystems

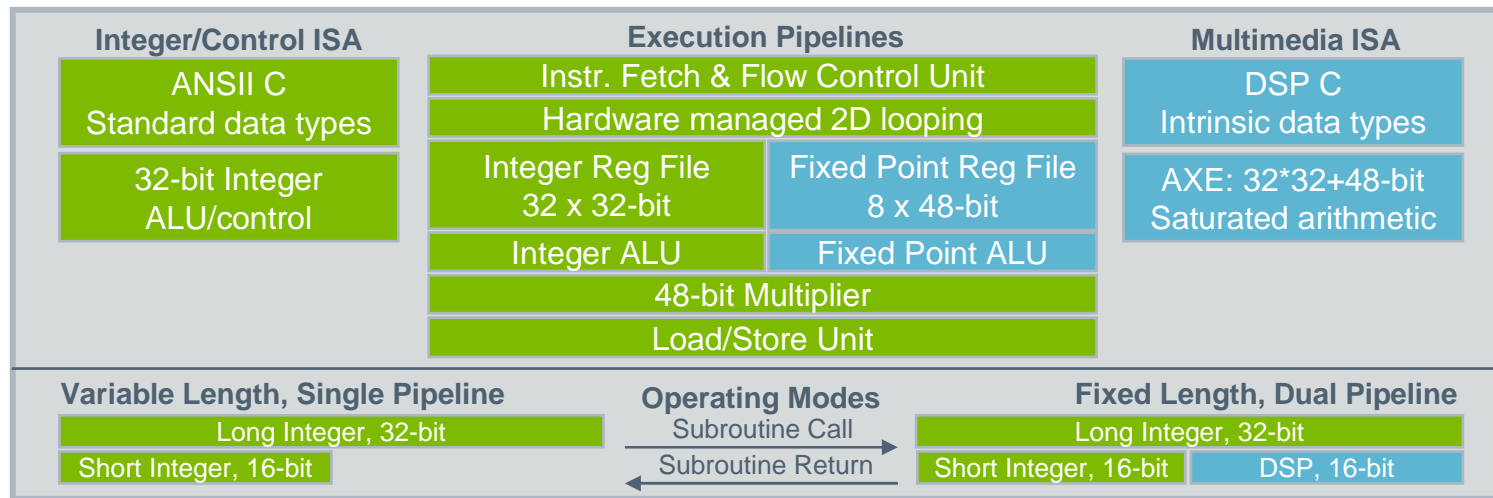
e300 Power Breakdown



e300 Performance Improvement



Multimedia Acceleration Core



- » Multimedia core optimized for audio applications
 - 32*32+48-bit saturated audio processing
 - 8K instruction cache, 2K instruction SRAM and shared 128K data SRAM
- » Software development
 - Available scheduler for multiple thread concurrent operation
 - Available audio acceleration tasks (e.g. sample rate conversion)
 - Available optimized full audio codecs (minimal e300 codec overhead)
 - Third parties porting algorithms to offload real-time e300 audio processing
- » Not limited to audio applications
 - C compiler, linker and hardware debugger code development environment
 - Integration is capable to perform enhanced DMA tasks

Multimedia Acceleration Core Performance

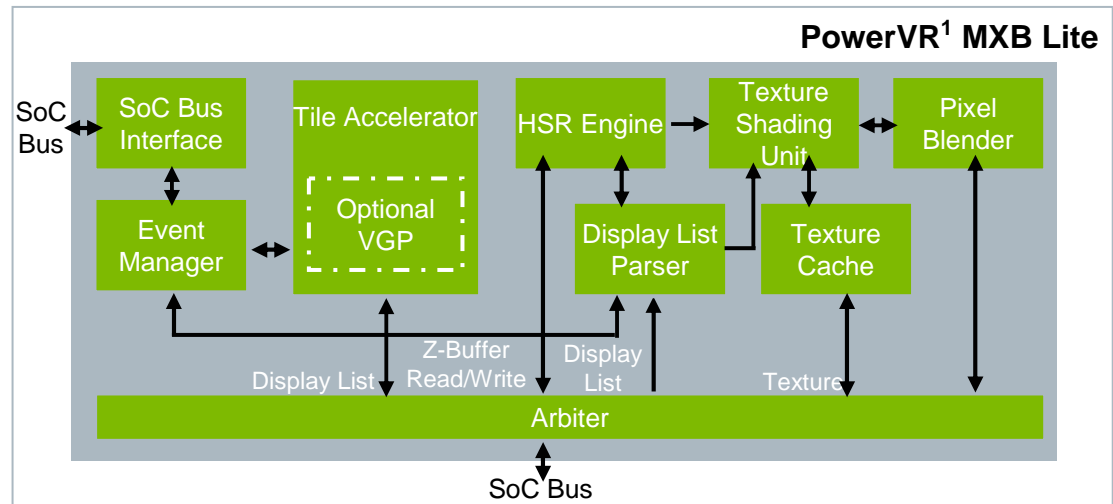
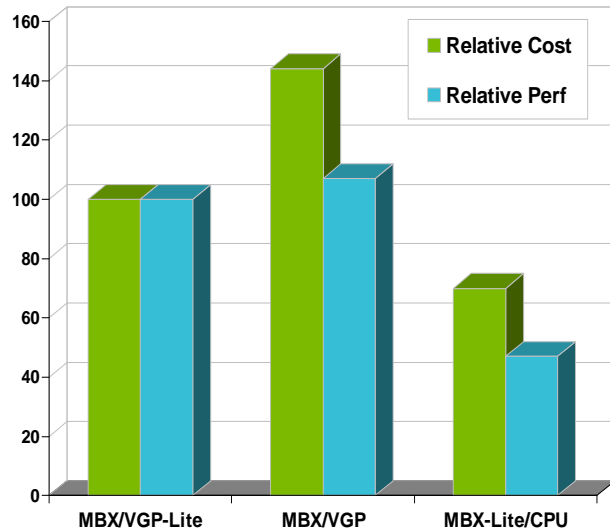


- » Performance numbers are based on production-level codecs developed for the acceleration core.
- » Actual performance will fall somewhere between the demo sys as an lower bound and simulator as an upper bound on performance.
- » On-chip SRAM usage by the codecs has been optimized to consume SRAM from the total at same rate as performance for concurrent operation.
- » e300 comparisons are estimates.

- 1.) Measured on demo platform system
- 2.) Cycle accurate C simulator with ideal memory
- 3.) FPU based estimates

Application	Avg MHz ¹ (demo sys)	Avg MHz ² (simulator)	e300 MHz ³ (estimate)	Tested Format
Audio Decoders				
MP3	7.3	6.9	20	128 kbps, 44.1kHz, stereo
	9.1	9	21	320 kbps, 48 kHz, stereo
MP2	4.4	4.3		128 kbps, 44.1kHz, stereo
	5.3	5		384 kbps, 48 kHz, stereo
AAC (w/ PNS & TNS)	10.7	8.5	33	128 kbps, 44.1kHz, stereo
	14	11.1	35	320 kbps, 48 kHz, stereo
WMA	9.5	7.8	45	128 kbps, 44.1kHz, stereo
	12.7	10.5	51	320 kbps, 48 kHz stereo
Ogg Vorbis	20	15	55	0.6 quality, stereo
	28	22	61	1.0 quality, stereo
Audio Encoders				
MP3	32	27	40	128 kbps, 44.1kHz stereo
	33.5	26.5		320 kbps, 48 kHz stereo
MP2	15.3	14.5		128 kbps, 44.1kHz, stereo
	16.6	16		384 kbps, 48 kHz, stereo
Ogg Vorbis	28.5	21		VBR 0.6 quality, stereo
	35	24.5		VBR 1.0 quality, stereo
Video Decoders				
MPEG4 SP	4.5	3.2		MHz/frame, XVID player
QVGA	3.7	2.7		MHz/frame, FFmpeg library
Other Algorithms				
SRC	5.8	5		44.1 kHz stereo to 48 kHz stereo
any-any rate	11.4	10.6		44.1 kHz stereo to 8 kHz stereo

2D/3D Graphics Acceleration Core



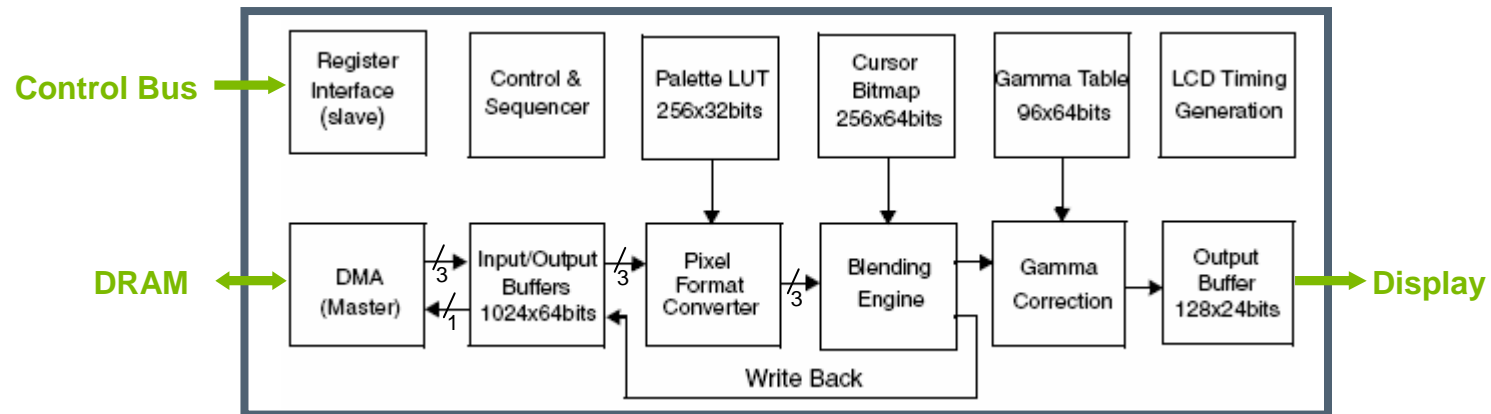
» Key features

- 100MHz MBX/VGP-Lite integration
- Fill rates exceeding 135Mpixels/sec² & 1.7Mtriangle/second throughput
- Tile-based deferred rendering with on-chip buffer to minimize memory bandwidth
- Complete OpenGL-ES1.1 3D graphics feature set with full screen anti-aliasing

» MPC5121e implements best cost/performance option

- 1.) PowerVR is a family of graphics engines developed by Imagination Technologies
- 2.) Effective fill rate assuming a depth complexity of three
- 3.) MBX-Lite/CPU assumes a 533MHz CPU to perform the VGP calculations
- 4.) MPC5121e integrates a 100MHz MBX/VGP-Lite configuration

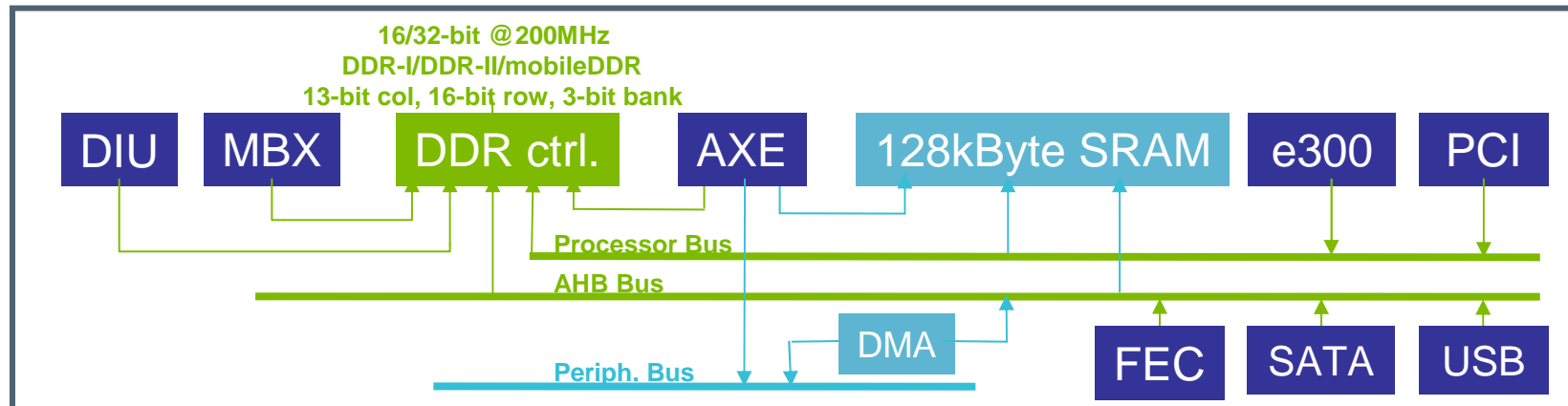
Display Interface Unit (DIU)



» Key features

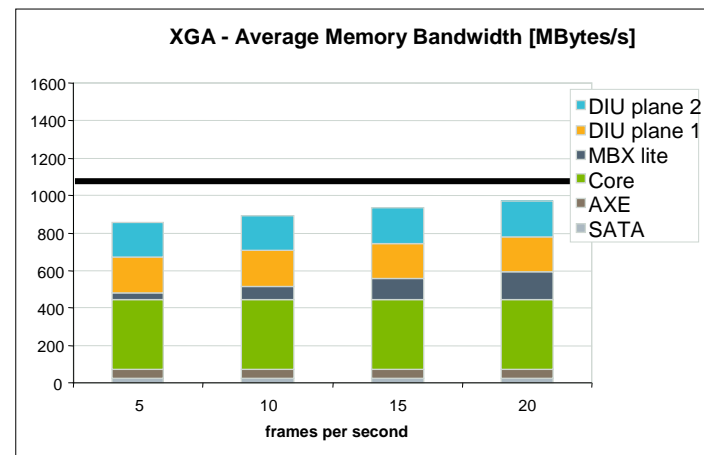
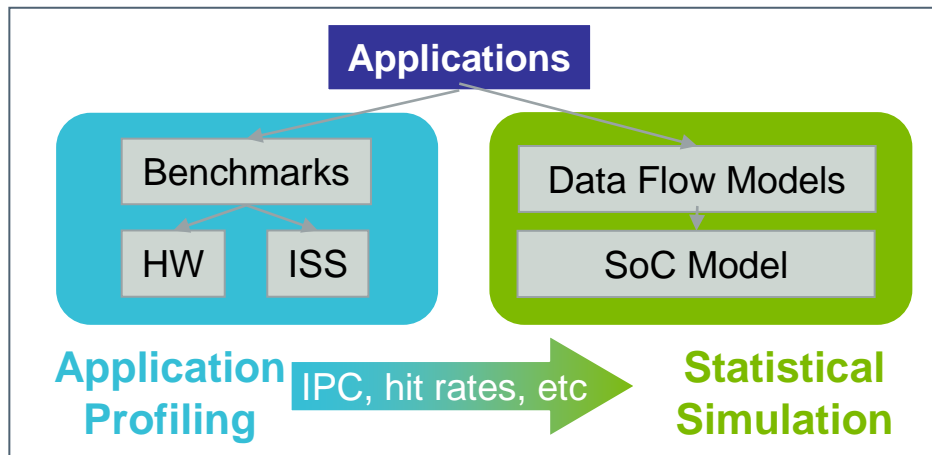
- 3-plane alpha/chroma key blending supporting up to 66Mpixels/sec
- Blend write-back to DRAM to support lower rate N-plane blend
- Each plane can be build from multiple sub-planes using area descriptors
- Color conversion to α RGB 8:8:8:8 from many pixel formats including 8-bit palletized
- Generation and blending of a 32x32 pixel animated cursor
- Gamma color correction and 24-bit RGB display output
- Full dynamic clock gating during idle processing time

Multi-Client DRAM Controller



- » Multi-core architecture sensitive to DRAM throughput/latency
 - Unified memory multimedia architectures demand high throughput
 - Computational bandwidth affected by cache miss stalls (e.g. e300, acceleration core)
 - Must prevent computational failure on real-time accesses (e.g. DIU)
 - Bandwidth wasted by page thrashing, read/write exchange and poor burst patterns
- » Arbitrated low latency multi-client controller architecture
 - 160-byte posted write buffer to reduce read/write transitions
 - Command arbitration (high->low: read, write, activate, precharge) across client accesses
 - Default priority given to open page, hidden precharge/activate on waiting client access
 - Support for 8 concurrently open pages to reduce page thrashing
 - Repeated long burst support on clients to maximize sequential access page hits
 - Architecture optimized for 16/32-byte burst sizes with critical word first wrapping
 - CAS+3 hit and CAS+6 miss cycles of read latency on priority client accesses

Architectural Bandwidth Simulations



Simulated Maximum Throughput

1100MBs (70% theoretical)

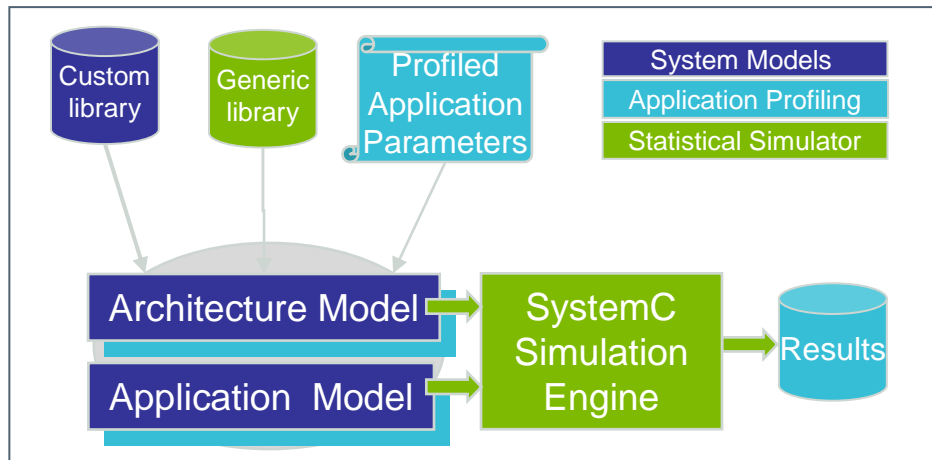
Application model with max graphics frame rate

Application Model:

- 4x mp3 encoding
- 1x mp3 decoding
- 15k triangles/frame
- 24-bit RGB color
- 60Hz XGA refresh

Architecture Model:

- 0.5 IPC
- 1% I-cache miss rate
- 2% D-cache miss rate
- 25% write back rate
- 50% load/store rate



Performance Monitors



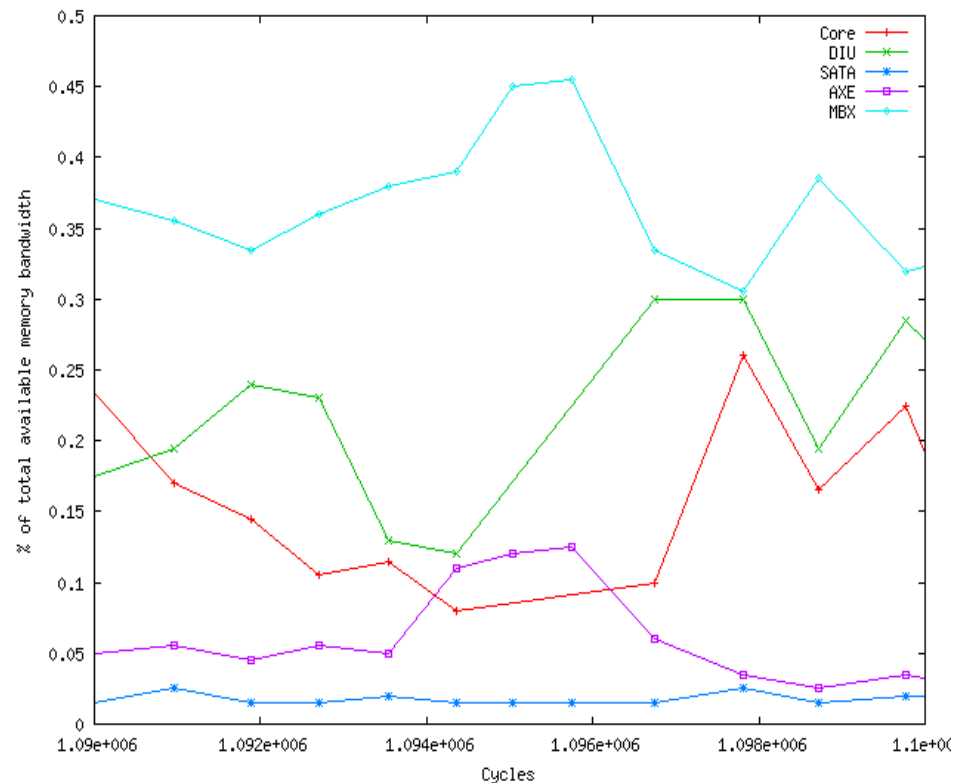
» Hardware statistical monitors

- e300 core
 - No. of read requests
 - No. of write requests
 - Address filtering supported
- DRAM clients
 - Memory bandwidth
 - Average latency
 - Average priority
- Capture mechanism
 - Memory mapped registers
 - Non-intrusive to application

» Post processing possibilities

- Periodic dump of statistics to external memory
- Process/visualize raw data using analysis tool of choice

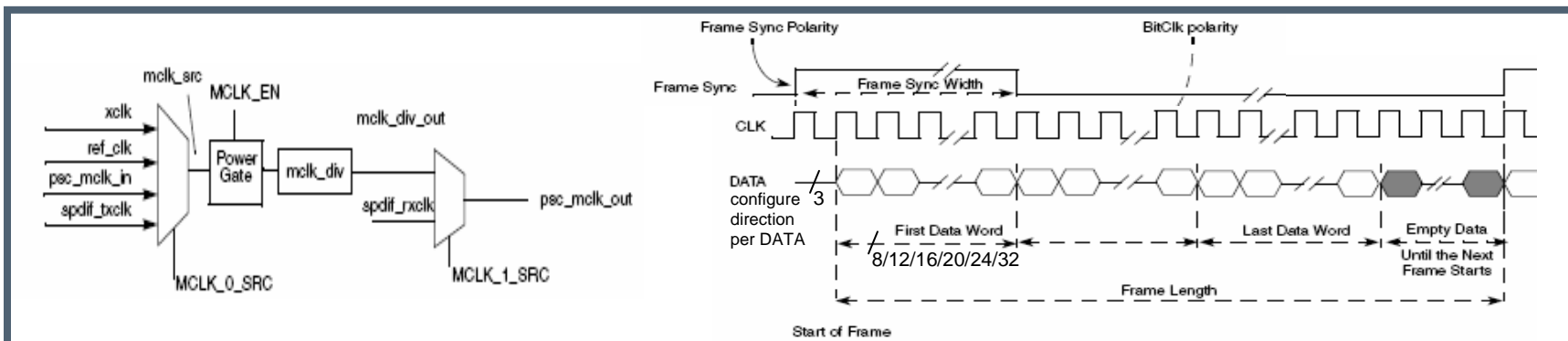
Example: memory bandwidth trace



System BOM Reduction



- » Considered following options for system “bill of material” reduction
 - Find non-commoditized functionality with acceptable integration complexity
 - Select package which achieves best trade-off between device & board cost
 - Minimize power consumption & high-speed requirements to limit package complexity
 - Consider flexibility to reduce overall device cost and address a wider set of applications
- » Programmable Serial Controller (PSC)
 - 12x 5-pin serial ports (UART, SPI, AC97, IrDA, multi-sample codec)
 - Subsets of total common FIFO can be allocated to each PSC Tx/Rx datapath
 - Chip selected SPI implementation can be achieved with GPIO programming
- » Clock synchronization
 - External clock reference sharing supported between all PSC and S/PDIF controllers to eliminate the need for sample rate conversion
 - 4-channel high accuracy long-term average clock frequency measurement



High-Speed Serial Integration



- » Analog integration challenges
 - Die area and power consumption costs
 - Signal integrity in low-cost wire-bond packaging
 - Significantly impacts development cost & time-to-market
 - Process technology selection impacted by available/planned analog IP

- » Hi-speed USB
 - 480Mbps single-channel high-speed OTG integrated PHY
 - Two OTG controllers to allow full host or device capability
 - Both controllers support 12-pin ULPI interface to external PHYs
 - CEA-936-A, Mini-USB Analog CarKit Interface compatible

- » Serial ATA
 - 1.5GHz single-channel integrated PHY
 - SATA-I controller supporting latest specification
 - No standard external PHY interface, alternative is PATA UDMA-5

Built on a Complete Ecosystem



» **Multiple RTOS providers**

- Wind River, QNX, Green Hills, and Linux

» **Middleware providers**

- ALT Software, Extended Systems, Gracernote, Tilcon, CSR, IBM, Engenuity, Nuance

» **Application providers**

- Lectronix, Tele Atlas

» **Enabling open source community**

- Freescale Auto Grade Linux (AGL) with real-time services, Denx

MPC5121e Multi-Core Summary



» Provides a new level of integration beyond the MPC5200

- Optimized for the telematics market
- Addresses a wide set of applications due to its integrated features, optimal power/performance and capability to withstand harsh operating conditions

» Foundation for next-generation mobileGT family

- Low-power device technology for balanced power/performance trade-off
 - Less temperature sensitivity
 - Less penalty for higher levels of integration
 - Power dominated by application controllable dynamic power
- Multi-core architecture to efficiently address performance demands
- Integration and packaging strategy targeted at system BOM reduction
- DRAM bandwidth to enable future convergence integrations

» Product can be leveraged for applications beyond automotive

- Covers a wide range of operating conditions with high-quality standards
- Telematics application is driving an interesting general-purpose feature set
- Low-power operation enables battery-powered applications
- Easier to drive automotive products into non-automotive applications than the other way around

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