

OTHER

Technical training is at the heart of the Power Architecture Developer Conference. The technical sessions, panels, and labs will capture a wide range of interests and applications, encouraging the cross-pollination of ideas and the exchange of technical know-how. The presentations have been organized by discipline.

This schedule focuses on the discipline **"Other."** These technical sessions include topics such as chip design practices to improve energy efficiency and reduce waste; tutorials on the Power ISA and a proven, automated tool for validating architectural compliance; and general overviews on Power Architecture processors and SoCs from multiple vendors. Additional topics will be covered that may be relevant to your business. To see the full schedule, go to <http://www.power.org/devcon/07/schedule/>.

Monday	Session
10:15 a.m. – 12:15 p.m.	Next Generation POWER Microprocessors (viable and expanding) - Panel
1:45 – 3:45 p.m.	Power ISA Tutorial <i>IBM</i>
Tuesday	
8:30 – 10:30 a.m.	Overview of Current Power Processor Standard Product Offerings - Panel
9:30 - 10:30 a.m.	Environmental Impact of Chip Design Practices <i>Cadence</i>
	Power.org Embedded Power Architecture Platform Requirements (ePAPR) Tutorial
10:45 a.m. – 12:45 p.m.	Power.org Technical Subcommittee Overview and Audience Feedback - Panel
12:45 – 1:45 p.m.	An Automatic System for PowerPC Architecture Compliance Validation <i>IBM</i>
	Multi-core Enablement - Panel

**QUESTIONS?
CONTACT US.**

E-Mail: PADCinfo@power.org
Phone +1-512-215-4831
<http://www.power.org/devcon>

To register, go to www.power.org/devcon.