

The Power Architecture Developer Conference offers 65+ hours of sessions, labs and panels covering a wide array of interests and applications. The following sessions are particularly applicable to your market segment. Additional topics will be covered that may be relevant to your business. To see the full schedule, go to <http://www.power.org/devcon/07/schedule/>.

## CONSUMER

Monday	Session
10:15 - 11:15 a.m.	WiMAX Based Solution for Infrastructure and CPE, <i>Freescale Semiconductor</i>
	Next Generation Multi-GHz Multi-Core Power Architecture CPU, AMCC
11:15 a.m. - 12:15 p.m.	Hybrid Multi-Processing with Embedded PowerPC 405 Cores in FPGAs, <i>Xilinx</i>
1:45 - 2:45 p.m.	PowerPC Embedded MMU and Cache Management, <i>Technonics, Inc.</i>
	Using Simulated Hardware to Debug Multi-core Software, <i>Virtutech</i>
2:45 - 3:45 p.m.	A Soft Computing Multi-core Solution for Image Restoration, <i>Sona College of Technology</i>
	Titan - An Ultra High-perf., Power and Area-efficient Core, <i>Intrinsity, Inc.</i>
4:00 - 5:00 p.m.	Virtualization Features of PWRficient 1682M, <i>P.A. Semi</i>
Tuesday	
9:30 - 10:30 a.m.	Design of 2GHZ High Performace Low Power Dual-core Processor, <i>P.A. Semi</i>
10:45 - 11:45 a.m.	Digital Video Processing with Power Architecture Technology, <i>Freescale Semiconductor</i>
	OpenEmbedded, <i>OP SIS</i>
12:45 - 1:45 p.m.	Hybrid Multi-core Debugging Solution on a Power Architecture™ Embedded Platform, <i>Freescale Semiconductor</i>
	Xen Hypervisor for Cell Broadband Engine, <i>Samsung</i>
1:45 - 2:45 p.m.	System Design with the P.A. Semi PA6T-1682M, <i>P.A. Semi</i>
	Sourcery VSIPL++ for Cell B.E., <i>CodeSourcery, Inc.</i>
3:00 - 4:00 p.m.	TCP/IP Acceleration in Cell Broadband Engine Based Platforms, <i>Aricent</i>
	High Performance Secure Embedded Computing for the Cell Broadband Processor, <i>IBM</i>

To register, go to [www.power.org/devcon](http://www.power.org/devcon).

**QUESTIONS?  
CONTACT US.**

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