



Power.ORG ™

**DesignCon09**

# **Power Architecture EcoSystem Solution Offerings**

**Fawzi Behmann, Chair Marketing Committee, Powr.org  
Director of Strategic Marketing, NSD, Freescale**

**February 5, 2009  
9:00am-3:00 pm  
Room# 212**

The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.



## Special Multi-company presentations on Power Architecture Multicore Ecosystem February 5<sup>th</sup>, room #212

<b>9:00 – 9:15</b>	<i>Introduction, Fawzi Behmann, Power.org</i>
<b>9:15 – 10:00</b>	<i>“Multi-core PowerPC Software Development using Virtualization”, by Frank Schirrmeister, Synopsys</i>
<b>10:00 – 10:45</b>	<i>“System-Level Power Estimation and Exploration”, by Maulik Patel, Cadence</i>
<b>10:45 – 11:30</b>	<i>“Using System Simulation for Multi-core Debug”, by Ross Dickson, Virtutech</i>
<b>11:30 – 12:00</b>	<i>“Migrating to Multicore: How and Why”, by Toby Foster, Freescale</i>
<b>Noon – 1:00pm</b>	<i>lunch</i>
<b>1:00 – 1:30pm</b>	<i>“Freescale Power e200 IP Licensing” by Rick Tomihiro, IP Extreme</i>
<b>1:30 – 2:00pm</b>	<i>“ secure virtualization based on power Architecture” by Jack Greenbaum , GeenHills</i>
<b>2:00 – 2:30pm</b>	<i>“ Multicore and Hypervisor” by Wind River</i>
<b>2:30 – 3:00pm</b>	<i>“Using the GNU Toolchain to Build and Debug Applications for Power Architecture Processors”, by Mark Mitchell , CodeSourcery</i>



**Power.org Introduction and Brief  
Market trends driving multicore  
architecture**

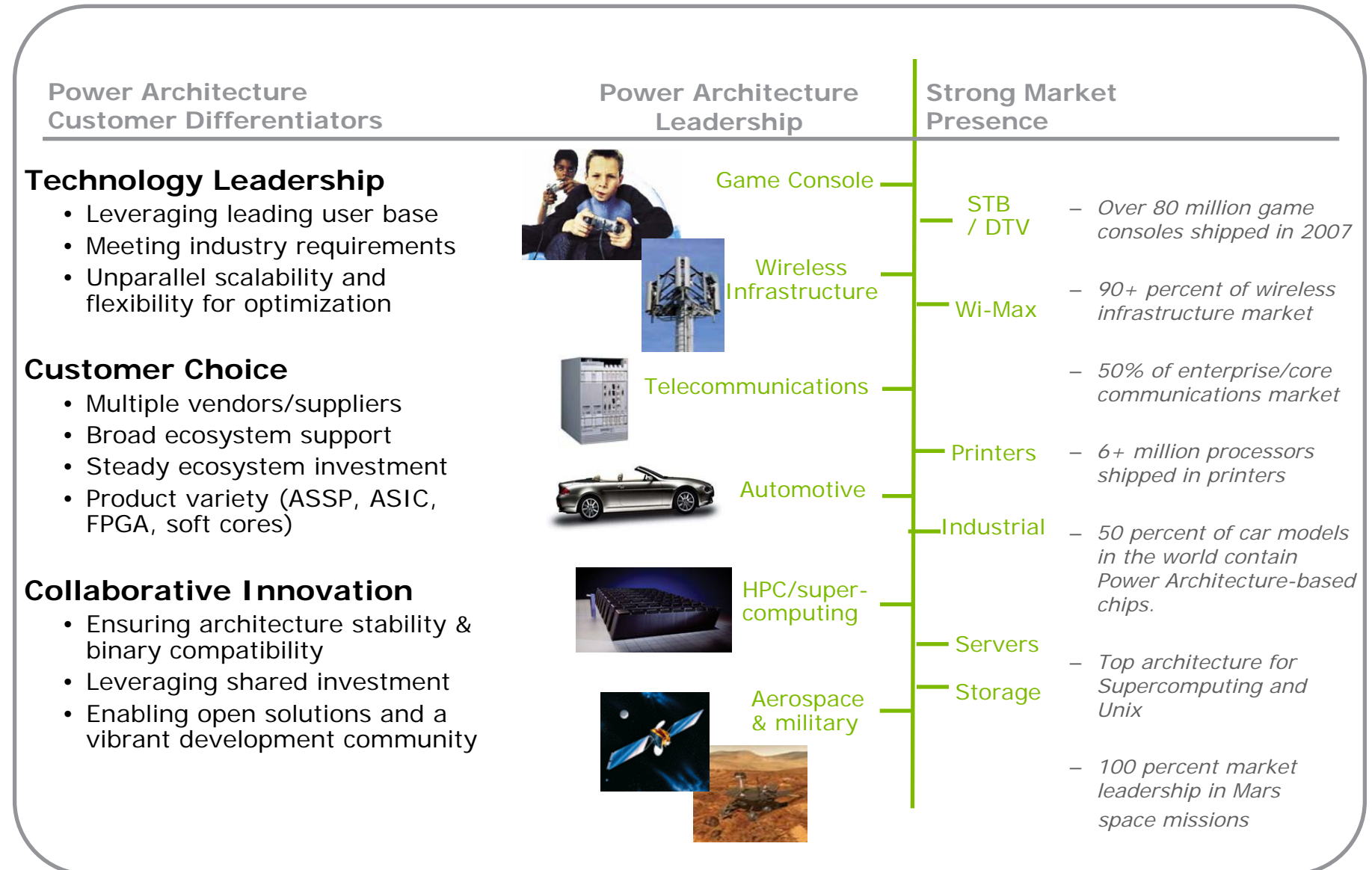
# Power.org stands for Collaborative Innovation

- » Power.org operates on the basic premise that collaboration among leading companies allows for breakthrough innovations
- » Power Architecture is open and allows choice of vendors and suppliers
- » Any company can OWN Power Architecture and build innovative solutions
- » Power Architecture is the most scalable architecture
  - Proven implementations from smallest devices to largest supercomputers
  - Has held world records in performance and innovations for 18 years
  - The ONLY architecture with proven reliability and scalability to have been used in ALL space missions to Mars
  - Leader in Multicore and Virtualization
    - Introduced in 2001, five years ahead of competition

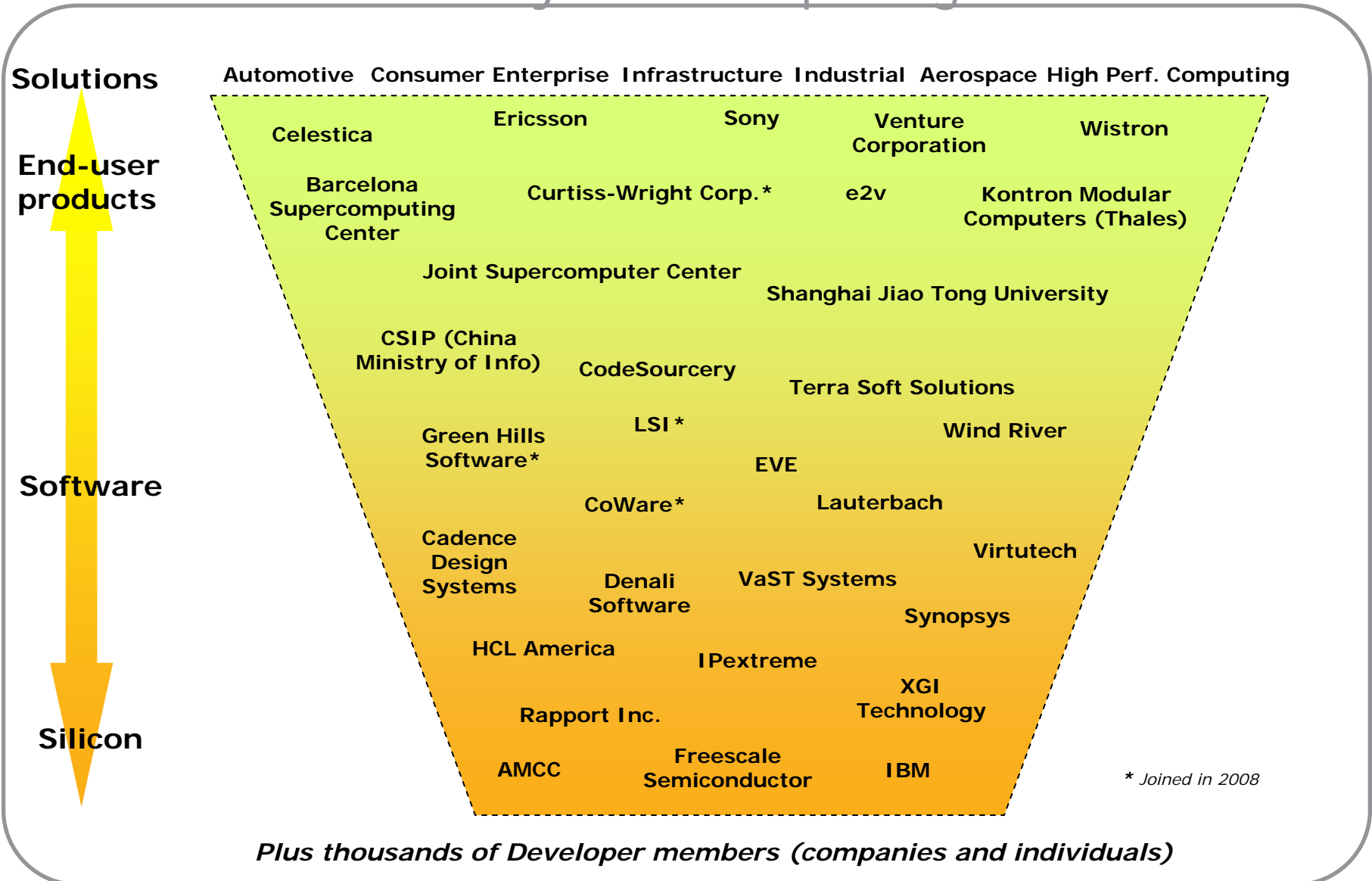
## Vision

***“The leading architecture in tomorrow’s connected world”***

# Power Architecture® Value Yields Leading Innovation

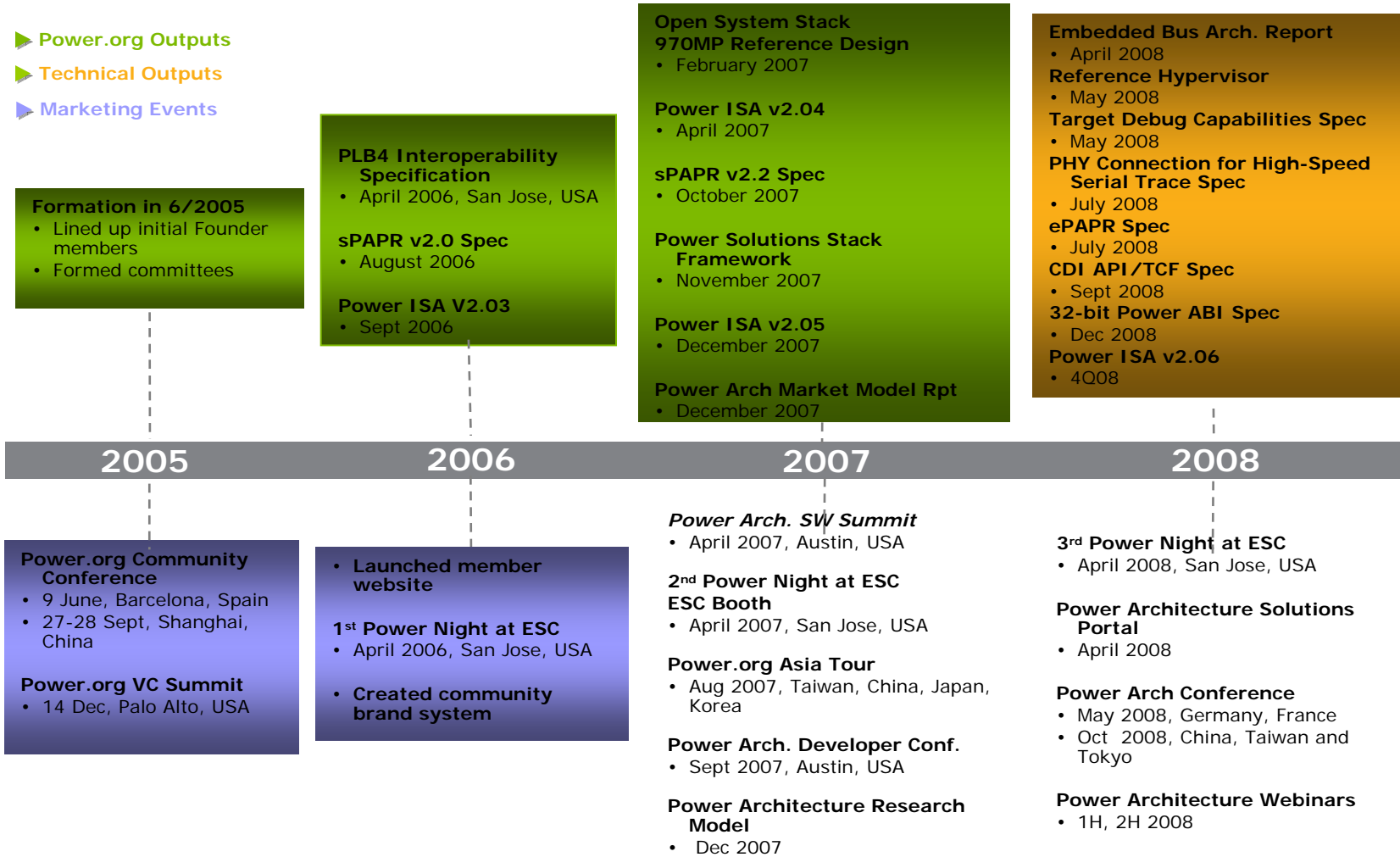


# Power.org's corporate members driving Collaborative Innovation and Ecosystem compelling solution



# Power.org's Power Architecture key milestones to date

- ▶ Power.org Outputs
- ▶ Technical Outputs
- ▶ Marketing Events



# Power.org Technical Subcommittees and Workgroups

## PAAC



**Objective:** Provide a collaborative environment to develop recommendations to IBM for Power ISA changes and evolution. Manage ISA specification's public release roadmap.

**Members:** IBM, Freescale

## Platform Arch



**Objective:** Define durable interfaces for the embedded platforms based on P.A. to lower the cost and increase the availability of SW.

**Members:** AMCC, Cadence, Ericsson AB, Freescale, IBM, IPextreme, P.A. Semi, Thales, Wind River

## Common Debug Interface



**Objective:** Define a common set of debug interface options that cover end to end debug tool chain for use in P.A. implementations.

**Members:** AMCC, Ericsson AB, Freescale, IBM, Lauterbach, National Instruments, VaST, Virtutech, Wind River, Xilinx

## Power ABI



**Objective:** Create unified ABI documents under neutral licensing that reflect the merged Power Architecture specification and existing coding standards (documented and undocumented but implemented)

**Members:** CodeSourcery, Freescale, IBM, Wind River

## Embedded Hypervisor



**Objective:** Develop a hypervisor optimized for embedded systems that takes the leadership virtualization knowledge of Power Architecture into the Book-IIIe domain.

**Members:** AMCC, Ericsson AB, Freescale, IBM, Linuxworks, MontaVista, P.A. Semi, Virtutech, Wind River

## Virtual Platform & Simulation



**Objective:** Integrate the relevant standards from OSCI, SPIRIT, and Accellera to enable best of breed ecosystem with virtual platforms to support pre-silicon system design and optimization.

**Members:** Freescale, IBM, Synopsys, VaST, Virtutech, CoWare, GreenHills

## Software Initiatives



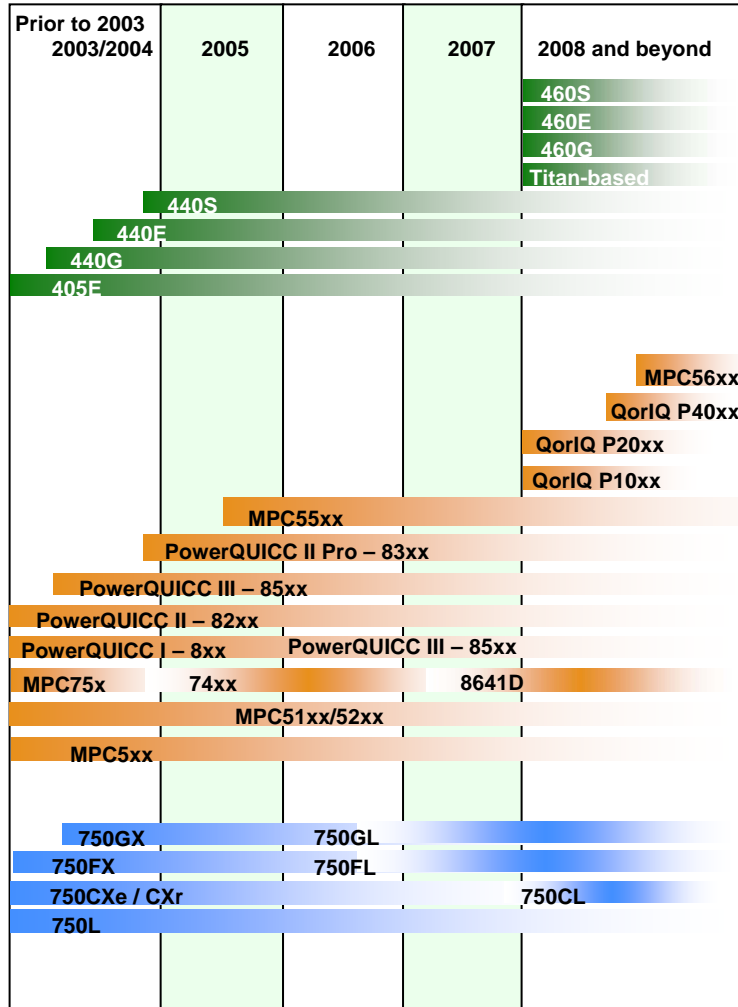
**Objective:** Identify gaps and initiate projects that enhance the ecosystem supporting OS, tools, middleware, and Applications on Power Architecture

**Members:** AMCC, Ericsson AB, Freescale, IBM, Lauterbach, P.A. Semi, VaST, Virtutech, Wind River, XGI

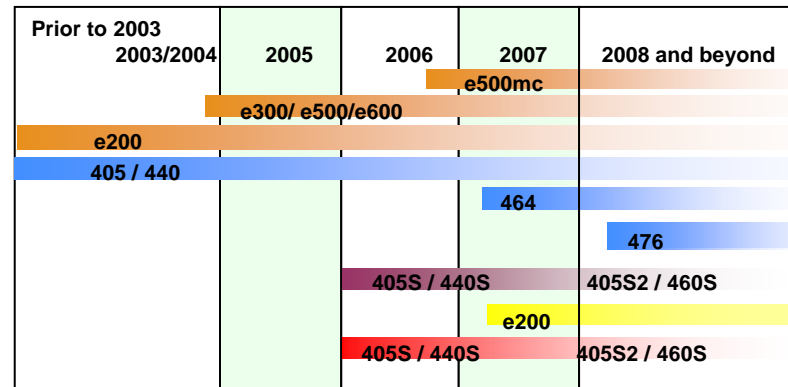
# Power Architecture® Silicon Roadmap

■ AMCC   
 ■ Freescale   
 ■ IBM   
 ■ HCL Technologies   
 ■ IPextreme   
 ■ Synopsys   
 ■ Xilinx

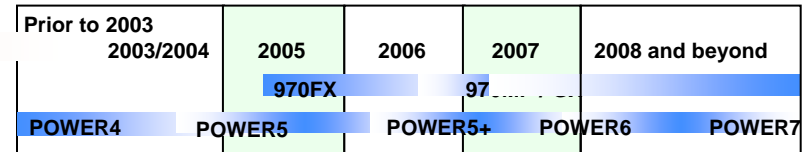
## 32-bit Commercial Processors



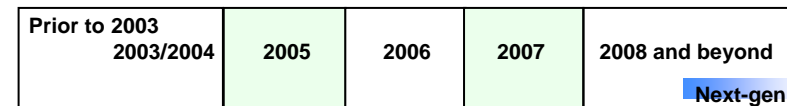
## 32-bit Commercial Cores



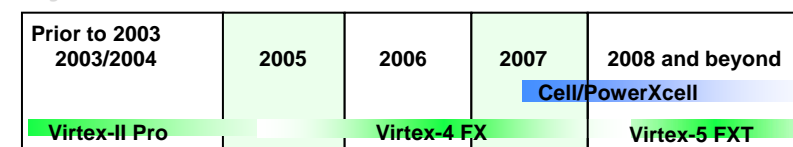
## 64-bit Commercial Processors



## 64-bit Commercial Cores



## Hybrid or Accelerator Architectures



# Collaborative Innovation of Power Architecture based on market and technology trends

Advancements of technology (video, wireless Broadband modulation, Scalable IP) and implementations are driving growth in high rich content broadband traffic

Future applications are demanding higher performance and increase in bandwidth on and off the chip

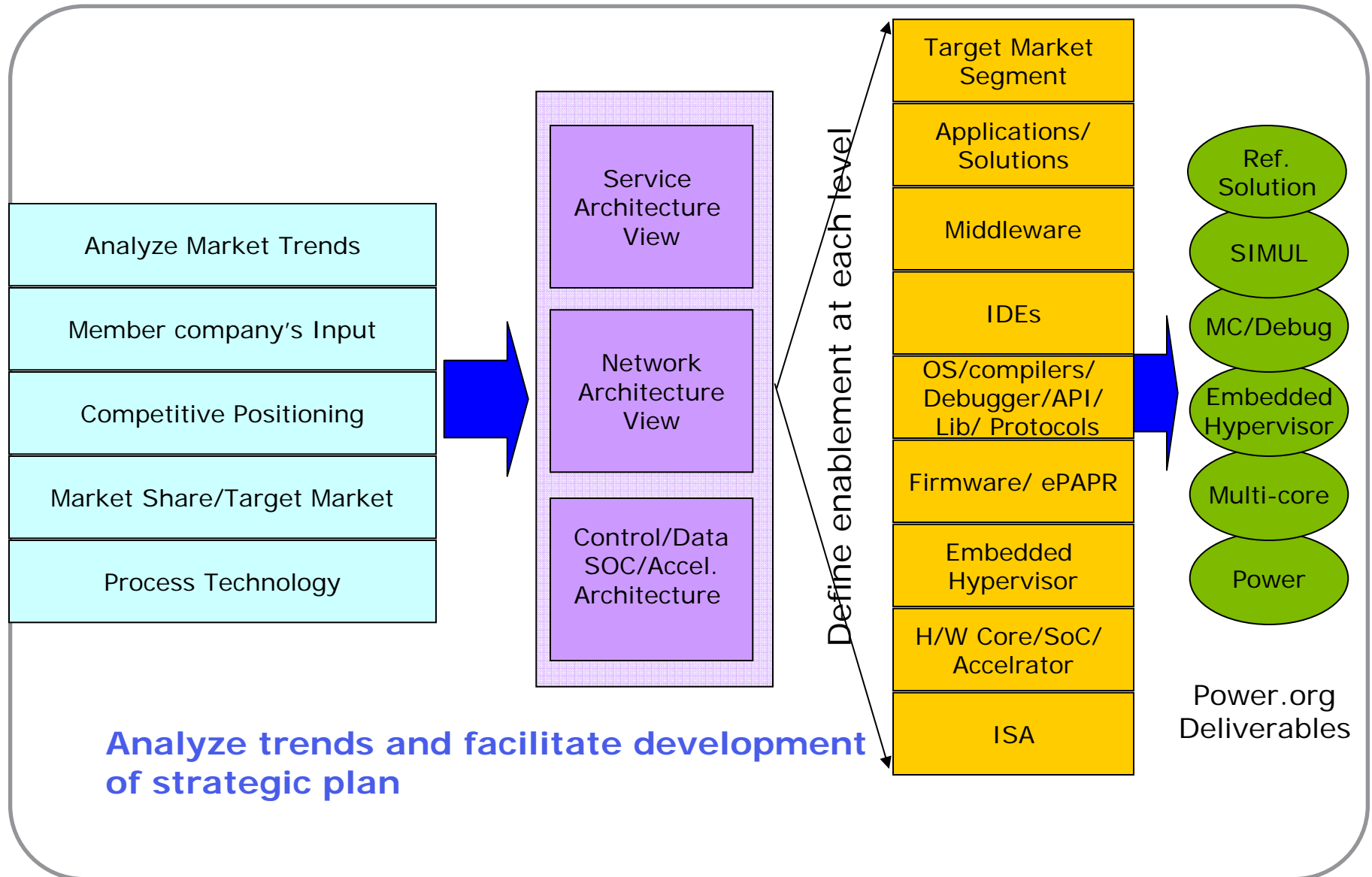
Low power requirements continue to be critical because of the growth of mobile devices and mobility

Advancement of new services and demand for service profitability are driving network migration and lowering CAPEX/OPEX

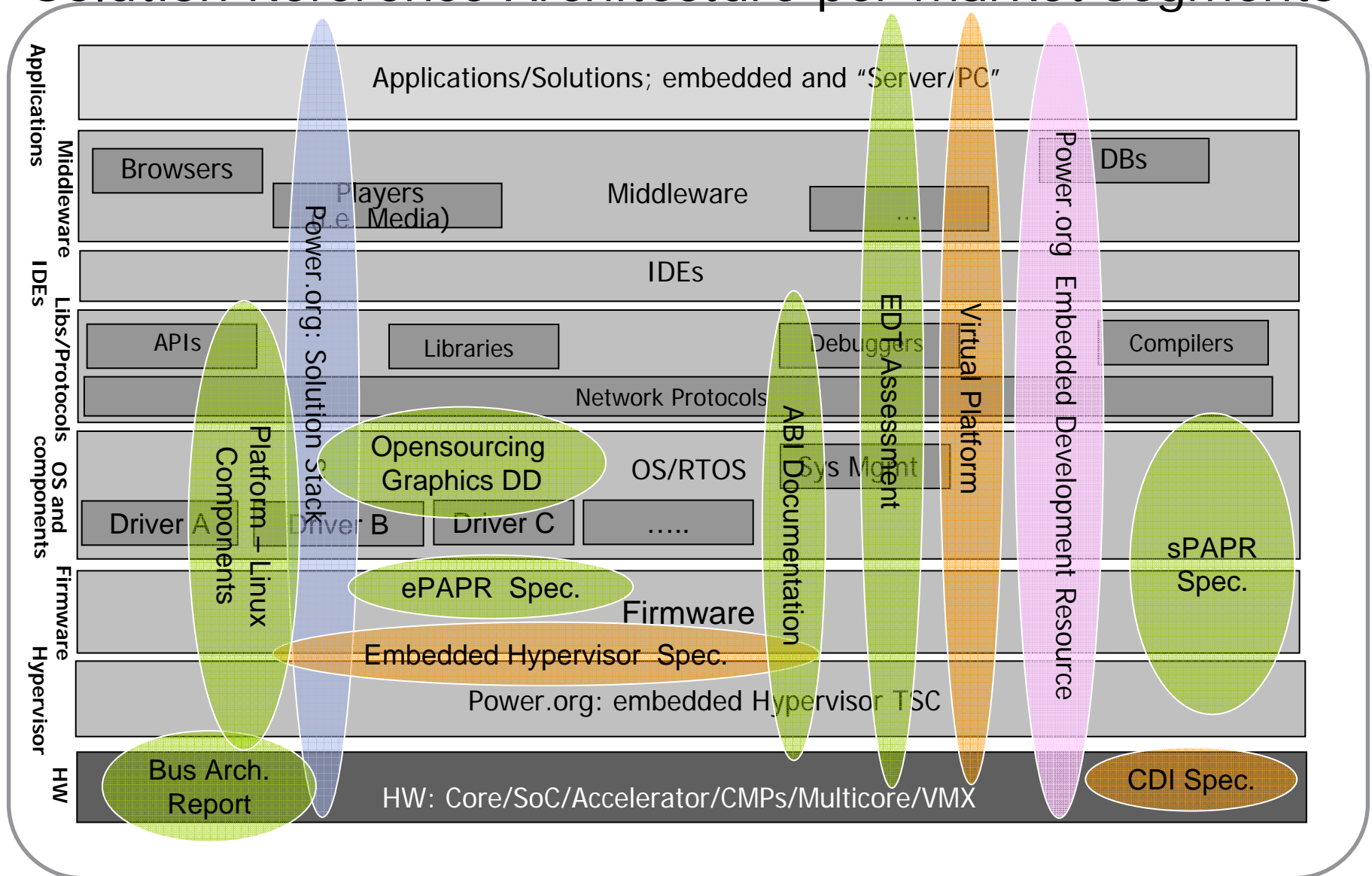
Multi-core architectures growing in order to support converging services and devices

Advancement in process technology and demand for higher performance/Hz/Watt demand SoC design, software programmability.

# Mapping future trends to focused activities







# Power Architecture Enablement and Interoperability Solution Reference Architecture per market segments



# The Power Brand System

The Power Brand Identity System represents a “platform brand” encompassing a number of product brands:

- POWER5,
- POWER6, etc.
- PowerPC
- PowerQUICC
- QorIQ
- Hybrid processing devices
- Cell Broadband Engine/PowerXCell
- Many unbranded families of SoCs and synthesizable core products

Master brand	 <p>Conveys “sum of all the parts” for this world-class technology platform, encompassing the instruction set architecture represented by the Power ISA and PowerPC ISA specifications, community, Power-compatible products and the wider ecosystem of companies and their solutions for this technology and its products.</p>
Organization affiliation brand	 <p>Identifies those organizations that are official members at the Founder, Sponsor and Participant levels.</p>
Solutions endorsement brands	<div style="display: flex; justify-content: space-between;"> <div data-bbox="772 732 1312 959">  <p>Identifies cores, processors, hardware and <u>computer systems</u> of any type that include and are 100% compatible with the core Power Architecture technology.</p> </div> <div data-bbox="1394 737 1892 1149">  <p>Identifies complementary products specifically designed for use with or usable with and services rendered in developing, building or maintaining cores, processors, and hardware and computer systems of any type that include and are 100% compatible with the core Power Architecture technology.</p> </div> </div>

Visit [www.power.org](http://www.power.org) for more information

# Summary and Value Proposition

## » Collaborative Innovation of ISA

- Selective evolution
- Based on market/technology trends

## » Enablement and Interoperability

- Based on Standards

## » Promotion of the brand and ecosystem

- Raise the tide for every member

## » Leveraged Investment Model

- Pool resources from members with tangible benefits for all
- Marketing & Technical collaboration
- Business Collaboration

## Power Architecture Ecosystem Solution offerings, room # 212

### Synopsys

» **Title:**

Multi-core PowerPC Software Development using Virtualization

» **Presenter:**

Frank Schirrmeister, 1-408-455-7290, fschirr@synopsys

» **Abstract:**

Design teams utilizing PowerPC embedded processors realize that hardware development is no longer on the critical path leading to chip volume production. With software development increasingly dominating the development effort, increased embedded software productivity and advancement of software development to earlier project phases have become crucial for product success. In addition, the rapid move to multi-core hardware platforms changes software development itself, nominally increasing the amount of processing performance but leaving developers puzzled as to how to distribute software across multiple processors. This presentation will illustrate the major issues causing lower embedded software development productivity for PowerPC based multi-core designs. It will introduce the concept of virtual platforms for virtualization of PowerPC multi-core hardware and illustrate how virtualization increases software development productivity by providing never before seen visibility into and control over the target hardware executing multi-core software.

## Power Architecture Ecosystem Solution offerings, room # 212

### Cadence

» **Title:**

System-Level Power Estimation and Exploration

» **Presenter:**

Maulik Patel, Product Marketing Manager, 1-650-823-5349,  
[maulik@cadence.com](mailto:maulik@cadence.com)

» **Abstract:**

To create power-aware system, tests must be representative of the actual use case. Traditional approach (spreadsheet or simulation) may not be practical for most SoC designs, since running software significantly impacts simulation performance. Cadence Palladium III Dynamic Power Analysis (DPA) solution uniquely enables engineers analyze impact of software within the system-level SoC architecture, and perform trade-offs between power and performance in a realistic system-level environment so design is power-aware.

## Power Architecture Ecosystem Solution offerings, room # 212

### Virtutech

» **Title:**

Using System Simulation for Multi-core Debug

» **Presenter:**

Ross Dickson, 1-617-504-1184, [dickson@virtutech.com](mailto:dickson@virtutech.com)

» **Abstract:**

When shifting to multi-core based systems the embedded software developer is presented with a range of new development and debug challenges. This presentation reviews the most common forms of the new challenges and shows how a Virtutech Simics Virtualized Software Development environment can simplify the task of addressing them.

Additionally best practices in multi-core software development are discussed.

## Power Architecture Ecosystem Solution offerings, room # 212

### Freescal

» **Title:**

Migrating to Multicore: How and Why

» **Presenter:**

Toby Foster, Systems Architect, 1-408-891-9778, [toby.foster@freescal.com](mailto:toby.foster@freescal.com)

» **Abstract:**

“Everyone agrees that multicore devices are part of the solution to address increasing performance requirements within fixed power budgets. But it remains a complex topic, with various possibilities around the number of cores and types of cores to use as well as how to use them. This discussion will describe the use cases and target applications for multi-core processors, and help shed light on what sort of multicore makes the most sense for what sort of application. We will review how chip-level architectures can either be intrusive or transparent to software, and look at how Freescal’s next generation of QorIQ multicore devices make multicore adoption easier.”

## Power Architecture Ecosystem Solution offerings, room # 212

### Wind River

» **Title: Wind River Multicore and Hypervisor**

» **Presenter: TBD**

Contact: Glenn Mortland, 1-512-527-4099, [Glenn.Mortland@windriver.com](mailto:Glenn.Mortland@windriver.com)

» **Abstract (Draft):**

Whether for evolution, performance or partitioning reasons, it is frequently desirable to use virtualization in order to run more than one operating system within a single core or multicore system. Manual resource partitioning and collaborative resource utilization can result in fault propagation paths between operating systems. Using a hypervisor simplifies system configuration, enforces resource partitioning, contains faults and enables more than one operating system on a single core or multicore system. This presentation covers the motivations, challenges and benefits of such multi-OS systems.

## Power Architecture Ecosystem Solution offerings, room # 212

### GreenHills

» **Title:**

Green Hills secure virtualization based on power Architecture

» **Presenter:**

Jack Greenbaum, Director of Engineering, Advanced Products , 805-679-3190 cell, jackg@ghs.com

» **Abstract:**

Green Hills will present its uniquely secure virtualization for Power Architecture, based on the only EAL6+ certified secure RTOS in the world, Green Hills' INTEGRITY RTOS. With INTEGRITY designers can safely run legacy applications or use freely available infrastructure running in a guest OS such as Linux alongside native RTOS tasks that demand real-time performance, safety, and security.

## Power Architecture Ecosystem Solution offerings, room # 212

### IP Extreme

» **Title:**

Freescale Power e200 IP Licensing from IPextreme

» **Presenter:**

Rick Tomihiro , VP of Marketing, [rick.tomihiro@ip-extreme.com](mailto:rick.tomihiro@ip-extreme.com)

»

» **Abstract:**

Freescale Semiconductor, a founding member of Power.org and a driving force in the evolution of the Power Architecture since the original PowerPC, is the world's leading supplier of 32-bit controllers. Freescale's e200 family of Power Architecture cores are well proven in a range of embedded applications, including their popular MPC5500 series of automotive devices. Those same e200 cores are now available from IPextreme, enabling any SoC or ASSP designer to benefit from the Power Architecture.

- » This presentation will cover the features, ecosystem and licensing models for the Freescale e200 family of semiconductor IP from IPextreme

## Power Architecture Ecosystem Solution offerings, room # 212

### CodeSourcery

» **Title:**

Using the GNU Toolchain to Build and Debug Applications for Power Architecture Processors

» **Presenter:**

Mark Mitchell, Chief Sourcerer, 1-650-331-3385x713,  
[mark@codesourcery.com](mailto:mark@codesourcery.com)

» **Abstract:**

In this session, we will offer tips for using the GNU Toolchain effectively to develop applications for Power Architecture processors. We also will present enhancements CodeSourcery has made to the GNU Toolchain recently, including new CPU support in the GNU C/C++ Compilers, multi-process debug support in the GNU Debugger, and other improvements. Finally, we will discuss useful features for Power Architecture developers in Sourcery G++, CodeSourcery's complete C/C++ development environment based on the GNU Toolchain and the Eclipse IDE.