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THE INSIDER'S GUIDE TO MICROPROCESSOR HARDWARE

CHIPS, SOFTWARE, AND SYSTEMS

The 2004 Technology Awards Blend All Three

By Kevin Krewell {1/31/05-01}

Each year we look back at the technologies that were either revealed during the previous year or made a significant impact in that year. The list of earlier winners is quite diverse, ranging from the processor and system architecture of IBM's Power 4, to the EUV lithography

developments that promise to extend Moore's Law scaling beyond the limits of optical lithography (and well beyond the end of this decade), to the software architecture of Microsoft's Next-Generation Secure Computing Base and Intel's mainstream multithreading (Hyper-Threading). This year's candidates also mix hardware, software, and systems. Each clearly cannot exist without significant cooperative efforts in all three areas.

We see three technologies making a big impact during the next few years:

- The first is heavily threaded and multicore (beyond two) mainstream processors.
- Virtualization, available for many decades in mainframe servers from IBM, will make it to mainstream PCs in 2006.
- The Cell processor, being developed by IBM, Sony, and Toshiba at the STI Design Center, promises to be a new architecture optimized for broadband media and 3D graphics performance, but with uses beyond the game console.

Processors Get Thread-Rich

Radically threaded processors—Sun's Niagara, Cavium's Octeon, and others—will challenge software to keep up with the challenges of performance scaling by increasing thread parallelism. Although processors like Octeon can be programmed in a pipelined fashion, with each core performing one function on packet data and passing it to the next core



for further processing, that is not the optimum programming model, as each process step would need to be sized nearly identically. (The slowest stage would be the limitation on throughput.)

The challenge for these significant SoC designs moves well beyond the intricacies of the logic design and the balance of on-chip bandwidth and off-chip I/O and memory bandwidth. Once those are successfully overcome, the next

challenge is to design software that effectively utilizes the 16 to 32 threads available within the processors—and to do so within the constraints of Amdahl's Law (Gene Amdahl's statement on the limitation of program parallelism). Some tasks are naturally parallelizable, but the goals of the program environment will be to minimize events (such as memory locks) that can serialize execution.

The hardware will be rolling out in 2005–2006; now we have to see the response from software. In addition, multicore server processors need to deal with software licensing issues. A number of companies still license software per core, not per chip, making core-rich server processors more expensive to run code on (than single-core processors are).

Programs Live in a Virtual World

The move to virtual architectures will make systems more robust and scalable. Server data centers already know the advantage of virtualization, where multiple virtual computers, running various applications, can be run, deployed, and

Flubs of the Year—2004 Edition

Although the semiconductor business enjoyed a recovery from the post-bubble collapse of 2001–2002, not everyone was having a good time in 2004. Intel, in particular, had one of its most embarrassing years since the Pentium processor's floating-point math error (known by many as the "FDIV" bug) in 1995.

The winner of the Vaporware Award for 2004 is the Intel liquid-crystal on silicon, or LCOS, display chip. Intel touted it at CES 2004 and said it would be produced in 2004. It was first delayed and then finally canceled—all in one year. The LCOS chip just beat out the 4.0GHz Pentium 4 processor, which Intel executives also promised by early in the year only to toss aside later. At least, the Pentium 4 hit 3.8GHz and added extra on-die cache, which is good enough for practical purposes. After all, 4.0GHz is just a big round number, not some critical milestone.

The newest award would be the **Changing Business Model Award** for companies that have failed to make it as chip suppliers and are transitioning to intellectual property (IP) companies. The nominees and winners (tie) in this category are **Transmeta** and **Intrinsity**. Intrinsity has dropped out of the MIPS processor business and is focused on licensing its

unique Fast14 logic. Transmeta is running out of cash to continue pursuing the x86 notebook processor business and is now getting most of its revenue from LongRun 2 technology licensing. Transmeta could not build a big enough chip business to pay back the huge investment its backers made in the technology. Both companies have significant pools of IP they figure are still worth millions.

The **Facing Reality (Finally) Award** would go to **Sun Microsystems** for canceling the Millennium and Gemini programs. Sun was trying to build too many new processors at the same time and was facing a shrinking market for its processors. Fujitsu had some very capable and productive designers and it was best for the two companies to work closer together on SPARC processor design.

The **Déjà vu Award** would go to our high-performance embedded-processor winner, the quad-core **Broadcom BCM14x0** family of processors. Many people at the Fall Processor Forum noted that the Broadcom/SiByte presentation was the second time they saw this chip presented, as it had been originally presented at MPF'02 but never shipped. But, in this case, it's better late than never.

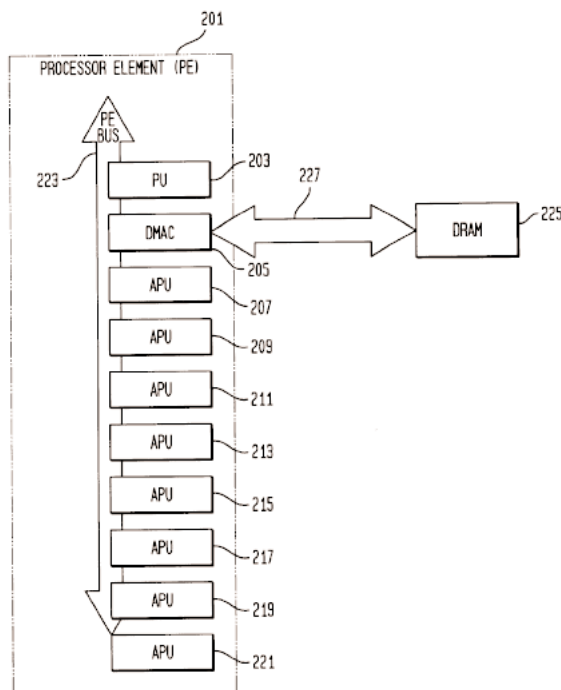


Figure 1. The basic block diagram of the Cell processor includes the processor element (PE) and eight attached processor units (APU). We now know that the PE is a PowerPC processor, and the APUs are 128-bit-wide SIMD engines. A DMA controller is responsible for data movement around the Cell processor. Source: U.S. patent 6,809,734.

managed on one or more physical machines. The range of virtualization technologies extends from the Hypervisor level (IBM term) that is very close to the BIOS and the kernel, to high-level Java and Microsoft.NET virtual machines in the application space. At the various levels in the software stack, virtualization has different effects on software.

The next wave of low-level kernel virtualization will take server functionality to desktop PCs. Intel's Vanderpool Technology and AMD's Pacifica Technology will allow multiple virtual machines to run on PC processors with greater efficiency than do pure software solutions (e.g., VMware). This will allow PCs to run multiple tasks and multiple operating systems concurrently, isolating critical tasks (digital video recording, for example) while other operations (like rebooting an operating system after a patch) can occur that could interrupt those operations. Both processor vendors are expecting to bring out this technology in 2006 to work with Microsoft's Longhorn operating system.

Another level of virtualization, below even that, is proposed by a company called Transitive Corporation. It claims to be able to virtualize processor instruction sets with a modest amount of overhead, allowing any operating system, ported to any processor, to be run on any other processor.

At high-level virtualization, Azul Networks can execute Java virtual machine code in a remote compute server. The company has built a custom SoC processor that will accelerate virtual machine architectures such as the Java VM. Here, virtualization allows workloads to be moved for different servers

and consolidated onto one server appliance that can execute JVM more efficiently than a standard server processor can.

These virtualizing technologies are possible because of the improvements in processor performance and the increases in transistor budgets. Processors are now fast enough that we can expend additional cycles on software productivity and protection. Hardware vendors are adding extensions to improve the speed and robustness of the virtual machine architectures, but they do not replace software. The results are a more flexible, adaptable, scalable, and reliable IT infrastructure.

Cell Starts Small, but Is Expected to Grow

The Cell processor has been kept largely under wraps by the development partners: IBM, Sony, and Toshiba. The joint venture by the three companies has pulled in resources from around the world and from many different disciplines to create a processor specifically designed to accelerate broadband (higher-bandwidth) media and 3D-graphics workloads. Emphasis in the design is placed on parallelism, with more SIMD (single instruction, multiple data) orientation, as the media and graphics data sets are amenable to SIMD operation. In these workloads, the same algorithm is applied to a large data set, and SIMD can prove very efficient. The initial target application for the Cell processor will be Sony's next generation game system, but the console will have capabilities beyond just playing games. In addition, the partners are talking about embedding Cell processors in everything from TVs to supercomputers.

Our story on the Cell architecture patents (see *MPR 1/3/05-01*, "New Patent Reveals Cell Secrets") gave us a look at the scope of the chip, if not the exact details of the implementation. What we know is that each Cell processor includes one multi-threading PowerPC core with multiple 128-bit SIMD streaming processor units. In the patent, there are a total of eight SIMD units.

More details of the architecture will be revealed at the ISSCC conference in February; at that time, we will have a detailed report on the architecture. The abstracts for the ISSCC papers seem to indicate that the processor is capable of clock frequencies that are more associated with high-performance PC processors. The main core of the design is a Power processor that is compatible with PowerPC, but with significant extensions.

The significant processing extension is an array of eight SIMD processing elements closely coupled to the Power core. With plenty of high-performance memory and I/O bandwidth, and with highly parallel compute resources running at multigigahertz speeds, the Cell processor is capable of supporting tremendous compute throughput. The design is also tied closely with a programming model and software support that can effectively use all these resources.

The Cell program combines a well-known high-performance core (PowerPC) with an array of compute resources, sophisticated data-movement support, and plentiful memory and I/O bandwidth. This mix is a recipe for a powerful product. The partners are busy building an ecosystem (an overused and abused word, but appropriate here) of software tools. Cell will be virtually guaranteed to be a unit-volume success when it ships in the next generation of Sony PlayStation consoles, likely sometime in 2006.

And the Winner Is...

With the promise of incredible performance and scalability, and what is basically a vector supercomputer on a chip, we present the 2004 *Microprocessor Report* Analysts' Choice Award for **Best Technology** to the **Cell Processor**. Congratulations to the STI Design Center and the participating employees at IBM, Sony, and Toshiba for what promises to be a very exciting challenge to mainstream processors. ♦

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