

Technical Committee Newsletter

3Q2007

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Greetings from the Chair

Team,

The September Power Architecture Developer Conference (PADC) is shaping up to be a first class event, thanks to the hard work of Kaveh Massoudian, Jesse Stein, Lovdy Hamm and others. I hope to see each of you at the PADC and have the chance to talk with you about current Power.org technical initiatives and our focus for 2008. Your contributions to our 2008 plan discussion are critically important to our collaborative approach and ensuring that our priorities are properly set.

Good progress continues to be made on the ePAPR and Common Debug Interface technical programs. New TSCs that were recently proposed include 1) Embedded Hypervisor and 2) Power Application Binary Interface. Additionally, the leadership team at VaST has taken the initiative to present to the SoC TSC and TC a concept proposal for enhancing the SoC / system modeling capability with Power processors. The SoC team is evaluating this proposal, which leverages VaST's technology, to decide if this should become part of the Modeling TSC charter/scope proposal under consideration. In addition, the team is looking at how to generalize the concept so that it encompasses component options from all interested member companies. If you want to be part of this discussion, please contact Nagu Dhanwada (IBM).

We have begun putting together a "solutions stack database" that will be added to our website. Member inputs are needed over the next few weeks. Please contact Joan Woolery if have content to add. The current database template can be viewed by visiting here: <http://www.power.org/apps/org/workgroup/tech/download.php/1636/latest>

Power.org membership and momentum continue to grow. Our unique open collaborative approach brings member companies value through your contributions. My thanks continue to go out to those who are actively contributing and showing leadership.

Sincerely,

Michael Paczan
Chairman, Power.org Technical Committee
tech-chair@power.org

Urgent News & Member Announcements

- **Power.org hosts the first-ever Power Architecture™ Developer Conference September 24-25, Austin Convention Center, Austin, Texas**

Be there when we kick off the first ever Power Architecture™ Developer Conference, the only industry event to showcase the full depth and breadth of the amazingly versatile Power Architecture technology. The technical program discloses new information on software development for the Power Architecture platform, multi-core solutions, virtualization compute-intensive solutions, and digital media, as well as an embedded perspective. Presenting companies include AMCC, CodeSourcery, Inc., Denali Software, Inc., EEMBC, Freescale Semiconductor, GE Aviation, Green Hills Software, IBM, Intrinsity, Inc., IPextreme, Mentor Graphics, Mindtree Consulting Ltd, OPSIS, PA Semi, Sona College of Technology, Technonics, Inc., Thales Computers and other members of the growing Power.org community.

As if 65+ hours of labs, technical sessions and panel discussions weren't enough, Power.org has paired with Terra Soft Solutions, to add yet another exciting element to the program. The recently announced Cell Hack-a-thon II, a four-day event beginning two days before the Power Architecture Developer Conference, is a hands-on workshop in which six Sony PlayStation 3 consoles are concatenated into a supercomputing cluster. The Cell Broadband Engine, the innovative Power Architecture processor inside the PlayStation 3, has been dubbed a "supercomputer on a chip." Participants in the Cell Hack-a-thon II will work on head node installation, compute node image deployment, and use of Torque and Moab for job management. Participants will also be invited to test their own parallel (MPI) and distributed (Torque) code.

Member registration incentive program

Power.org is providing a special incentive where members can have their admission fees waived if they get 2 additional participants to register for the event. These additional participants must be external to their member company.

Who can participate? Any Power.org member employee

What do you need to do?

The Power.org member employee just needs to request a sales voucher code at PADCinfo@power.org and make sure to reference the Member Incentive Program. The requesting member would then circulate the voucher code to his/her colleagues, invite them to register and as soon as two register, s/he will be notified that s/he has qualified for a free conference registration and provided with a complimentary registration code.

- » Member registration incentive program:
http://www.power.org/devcon/07/register/mbr_incentive/
- » For more information about the conference or to look at the full schedule and session abstracts visit <http://www.power.org/devcon>
- » If you have not yet registered for the Power.org Developer Conference, visit <http://www.power.org/devcon/07/register/>
- » **Register with the Austin Radisson by August 23rd and get the Power.org rate.** Get details here: <http://www.radisson.com/power/>
- » Help us get the word out to your customers. Everything you need is at <http://www.power.org/devcon/07/sponsorship/sales>

- **New Power Source logo for Power Architecture tools, software and services**

Power.org is offering members the new Power Source logo to affiliate their companies' Power Architecture software, tools and services. The Power Source logo can be used on data sheets, marketing collateral, packaging or any other materials related to members' Power Architecture products and services in categories such as:

- » Development tools, systems or software
- » Test equipment
- » Software or applications
- » Chip design or manufacturing services
- » Programming services



As with most other Power.org trademarks, the new Power Source logo is licensed free of charge. Companies wanting to use the logo must 1) be members of Power.org [<http://www.power.org/join>] (Developer-level members qualify), 2) sign a Power.org Trademark License Agreement [http://www.power.org/brand_center/request/], and 3) offer a product and/or service “specifically designed for use with or usable with and services rendered in developing, building or maintaining cores, processors, and hardware and computer systems of any type that include and are 100% compatible with the core Power Architecture technology, specifically the standard instruction set architecture represented by the Power ISA or PowerPC ISA specifications.”

Companies already holding a Power.org trademark license automatically qualify for the new Power Source logo: the logos will be e-mailed to them from brand@power.org.

Please visit http://www.power.org/brand_center/home/ for more information or contact Tein Atkerson, the Power Brand Marketing Manager, at tein@power.org.

- **Power.org members hosted regional Communication Day in 4 Asia Pacific countries**

Hosted by IBM, Freescale Semiconductor, VaST Systems and Rapport, Inc., Power.org held the 2007 Asia-Pacific Communications Day events in Shanghai, Taipei, Tokyo and Seoul from 16 July to 27 July, 2007. These sessions provided Power Architecture education and ecosystem sales enablement to that region. Attendees had an opportunity to gain technology and Committee updates as well as forge face-to-face networking associations in an informative, easy-to-join forum. There were over 120 individuals in attendance across all of the events. Attendee feedback valued the rich content of the multi-member presentation material of Power Architecture and company capabilities. Feedback from the audience surveys suggested that similar Power.org sessions should be continued in region as a way of providing education and promoting opportunity identification for member companies. In addition, suggestions to improve enablement were also received and will be used as input in the 2008 Power.org planning about to get underway. A trip report can be found at: <http://www.power.org/apps/org/workgroup/mktg/>

- **Freescale opens licensing of Power Architecture e200 core family through IPextreme**

Extending the reach of Power Architecture technology in the embedded market, Freescale Semiconductor is licensing its e200 core family to designers of system-on-chip (SoC) devices and application-specific semiconductor products (ASSPs). Freescale will license its e200 cores, which are widely used in the automotive industry, through an agreement with semiconductor intellectual property (IP) licensing specialist IPextreme Inc.

“Licensing our Power Architecture e200 core family through IPextreme is a watershed development for the industry and our customers,” said Paul Grimme, senior vice president and general manager of Freescale’s Transportation & Standard Products Group. “This licensing arrangement will help further extend Power Architecture technology within the automotive industry and help to proliferate e200 cores into other markets, such as low-end, low-power embedded network applications. IPextreme is an ideal partner for this initiative

because they have successfully taken other key Freescale technologies, such as ColdFire® architecture and FlexRay™ technology, to market as licensable technology.”

IPextreme plans to market sell and support the synthesizable e200 cores to embedded designers who intend to integrate the cores into SoC or ASSP products targeting the automotive, industrial and low-end networking markets. The licensing initiative gives designers ready access to a full range of high-performance, low-power, small-footprint cores that are software compatible with the extensive Power Architecture installed base and that are supported by a large and growing ecosystem of development tools.

For more information about the Power Architecture e200 core licensing program, visit <http://www.freescale.com/e200licensing> or http://www.ip-extreme.com/IP/power_e200.html

- **Kozio, Inc. released new memory diagnostic options for automated DIMM SPD detection and ECC error injection testing**

Kozio, Inc., expert providers of automated hardware diagnostics ideally suited for interactive and automated board-level validation of devices incorporating Power Architecture technology, has released new memory diagnostic options for automatic DIMM SPD detection and ECC error injection testing.

If you have a new design using ECC SDRAM, the new ECC memory validation option tests and validates single bit error reporting. Kozio's ECC testing and verification includes:

- » Verifying that single bit errors are detected, corrected, and reported during reads to SDRAM memory.
- » Verifying that multiple bit errors are detected and reported during reads to SDRAM memory.
- » Verifying that single bit errors are detected, corrected, and reported during a read-modify-write sequence to SDRAM memory.
- » Verifying that multiple bit errors are detected and reported during a read-modify-write sequence to SDRAM memory.
- » Verifying that toggling every data bit in the memory word properly reports a single bit error.
- » Verifying that single and double bit errors are detected with different data words.
- » Verifying that single bit errors in more than one memory location are detected and reported.

If you are validating various DIMMs, kDiagnostics can now provide pass/fail results in minutes. It automatically reads SPD data from an SDRAM DIMM and performs SDRAM configuration. kDiagnostics™ is self-booting, ROM-based firmware. This automatic detection and configuration allows you to easily test any field-replaceable DIMM taking advantage of Kozio's comprehensive memory validation tests.

These new options are now available with Kozio's kDiagnostics product; a board-level validation tool used to quickly test and troubleshoot hardware issues.

Kozio provides high-performance automated hardware diagnostics for today's complex computing devices. Kozio software improves and streamlines current test methodologies and processes with proven, turnkey diagnostics for custom boards implementing processors from AMCC, Freescale and others. Kozio diagnostics can help throughout a product's lifecycle from validating new hardware in the lab and streamlining production test, to power-on self-test and automated returns testing. Kozio software reduces project schedule risk and development costs while increasing test coverage and end-product reliability. Kozio products are used by technology companies across the globe. For more information, please visit www.kozio.com.

- **New Members**

Welcome new members MontaVista and National Instruments to the Power.org family.

Technical Updates

Technical Committee

Our major TC meeting focus has been on two core items: 1) PADC preparation and 2) 2008 Strategy and Plans. Additional details are provided below.

Sincerely,

Michael Paczan
Chairman, Power.org Technical Committee

Objective: Establish and maintain the overall technical vision and goals for Power.org. Responsible for forming and supervising Technical Subcommittees (TSC) that develop reports, specifications and reference designs.

Chairman: Michael Paczan (IBM) [tech-chair@power.org]

Members: AMCC, Cadence, Chartered Semiconductor, Denali, Ericsson, Freescale, IBM, Mentor Graphics, Rapport, Silicon Application, Sony, Synopsys, Thales, Venture Corp, Virtutech, Wind River, Wistron, Xilinx

Meetings: Monthly conference calls. Quarterly face-to-face meetings.

Home page: <http://www.power.org/apps/org/workgroup/tech/>

Join group: <http://www.power.org/apps/org/workgroup/tech/join.php>

Group Status:

- The Technical Committee kicked off its 2008 planning cycle at the June face to face meeting:
 - Member contributions to this effort are requested and critically important to ensuring that the Power Architecture technical community is working on the top priority ecosystem issues in 2008. Work has been continuing at each monthly TC call.
 - The plan process description and key work areas for plan development were discussed and agreed to in June. The associated charts are available in the TC June meeting document folder: http://www.power.org/apps/org/workgroup/tech/documents.php?expand_folder_id=293#folder_293 . Look for further updates in each TC meeting Doc folder.
 - You can get directly involved in this planning effort by joining the monthly TC calls or by contacting Michael Paczan [tech-chair@power.org] to set up an individual call to discuss your inputs.
 - Fawzi Behmann reviewed the preliminary IDC Market Intelligence report with the Technical Committee at the June meeting. Another review will be scheduled on the IDC material when the study is complete.
- Work has started on creating a Solutions Stack template and database. The intent is two-fold. First by collecting information on viable solution stacks and the maturity of member and non-member company components that support them, we will identify ecosystem issues and gaps that the Power.org community potentially can help to address. Second, the goal is to add the Solutions Stack database to the Power.org website as an information tool to assist developers in understanding what is available to construct a solution for different areas. The current template/database can be obtained here:

<http://www.power.org/apps/org/workgroup/tech/download.php/1636/latest>

- Ed Angelovich is continuing his work on the "Developer Call Up Program" that will enable Developer level members to participate on Technical Subcommittees. The BoD review was positive and they support the proposal. We are evaluating how to make this proposal work from an operational (Web site/policy) perspective.
- New technical initiatives/proposals under development (please contact the listed leads if you have interest in participating):
 - Embedded Hypervisor TWG Lead: Hollis Blanchard (IBM).
 - Power ABI TWG Lead: Kate Stewart (Freescale).
 - Modeling and Simulation TWG Lead: Nagu Dhanwada (IBM).
- Recent TC decisions:
 - Charter proposals for the Embedded Hypervisor TSC and Power Application Binary Interface TSC were approved in June by both the TC and BoD.

Events:

- Developer Conference – 24-25 September, Austin, Texas.

Power Architecture Advisory Council

Objective: Discuss ISA contributions to the Power Architecture ISA and vote on whether to make recommendations to IBM regarding such ISA contributions.

Chair: Wolfram Sauer (IBM) [paac-chair@power.org]

Members: Freescale, IBM

Home page: <http://www.power.org/apps/org/workgroup/paac/>

Specifications:

- **Power ISA Version 2.04** (.pdf 7MB)
[\[http://www.power.org/resources/downloads/PowerISA_204-FINAL.Public.pdf\]](http://www.power.org/resources/downloads/PowerISA_204-FINAL.Public.pdf)
- **Power ISA Version 2.03** (.pdf 7MB)
[\[http://www.power.org/news/articles/new_brand/#isa\]](http://www.power.org/news/articles/new_brand/#isa)

Group Status:

- Power ISA Version 2.04 was approved by the PAAC and has been presented to the Power.org Technical Committee. It is now available to all Power.org members (see link above).

Key Deliverables:

- 4Q07 - Power ISA Version 2.05.

Bus Architecture TSC

The Bus Architecture TSC released an enhanced version of the PLB4 Interoperability Specification (PLB4 IOS v1.1) that incorporates the new DDR mode of PLB4, clarification of early burst terminations, and other updates. We are still working on improving the document’s visibility. It is important for developers of new PLB4 cores to understand that strictly adhering to the PLB4 IOS is the best way to ensure compatibility with existing PLB4 cores.

The Bus Architecture TSC is still gathering data on the low- and mid-performance buses in preparation for generating the Embedded Bus Architectures Report. It is still apparent that the CoreConnect and AMBA bus families must both be supported in order to meet the various requirements of embedded Power Architecture SoCs. The members will continue to investigate how to best incorporate both CoreConnect and AMBA cores into a single SoC.

A survey of the industry revealed that at least a few member companies are pursuing proprietary high-performance buses with hardware-enforced cache coherency. The thought is that these proprietary buses offer a competitive advantage that would be lost if a single high-performance bus was selected and used by all the member companies. However, the competitive advantage comes at a cost; the companies accept the fact that they will need to develop their own IP for CPUs, accelerators, memory controllers, and bridges to other buses. They will also need to develop their own verification IP, models and monitors.

The TSC is also interested in what ARM might come up with for its next generation bus. However, the members believe any follow-on to the AMBA family is not likely to offer the hardware-enforced cache coherency, synchronization, and atomic operations which are required or optimized for Power ISA.

The Bus Architecture TSC has and will continue to evaluate OCP-IP as a possible recommended interface. In theory, this would allow high-performance IP to be shared between member companies, who would then attach it to their proprietary bus via a bridge or gasket. However, OCP-IP is still in the process of defining cache coherent extensions, and these must be comprehensive enough to encompass all the proprietary buses being developed.

Sincerely,

Jason Hopp
Chairman, Bus Architecture TSC

Objective: Define a hierarchy of bus architectures and support structures to standardize the bus interconnect in Power based SoCs, enabling rapid reuse, lower development costs, and increased compatibility.

Chair: Jason Hopp (IBM) [barch-chair@power.org]

Members: AMCC, Cadence, Denali, Ericsson, Freescale, HCL Technologies, IBM, Mercury Computer, P.A. Semi, Synopsys

Meetings: Thursdays 12:00-1:00 PM EST

Home page: <http://www.power.org/apps/org/workgroup/barch/>

Join group: <http://www.power.org/apps/org/workgroup/barch/join.php>

Group Status:

- In the process of surveying the low-, mid-, and high-performance buses in the industry to generate an Embedded Bus Architecture Report

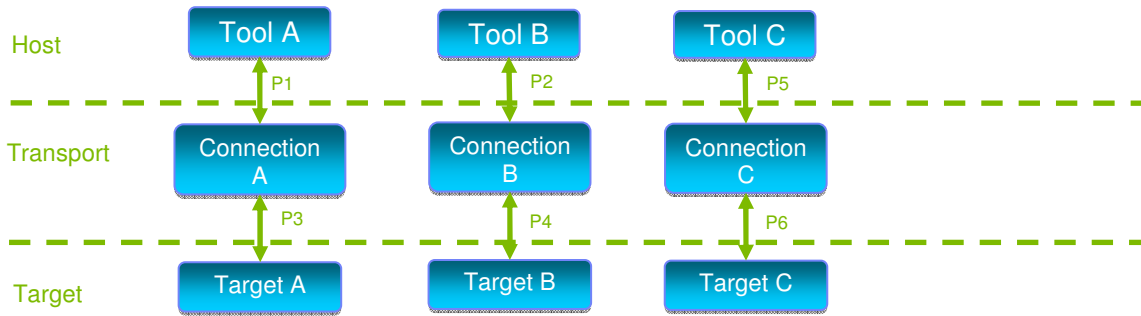
Key Deliverables:

• Vision and direction white paper	Complete
• Low-performance bus report	Complete
• Mid-performance bus report	Complete
• Updates to the PLB4 IOS	Complete
• Embedded Bus Architecture Report	3Q07

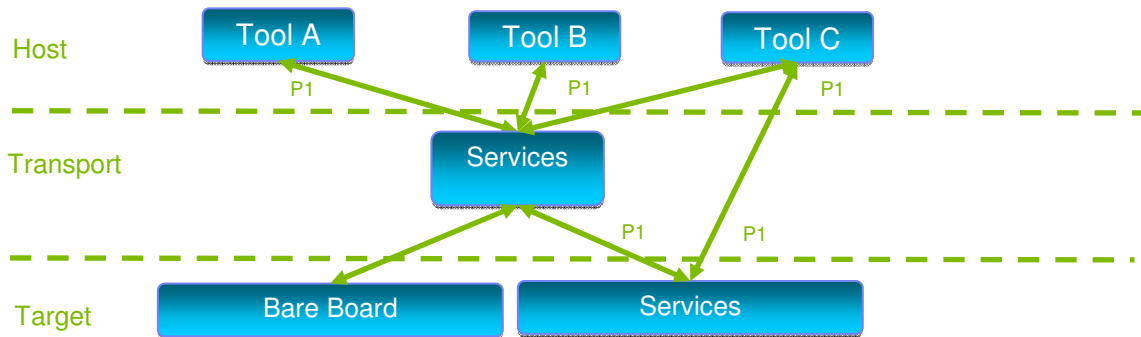
Common Debug Interface TSC

The three sub teams (API, PHY, TGT) within the Common Debug Interface TSC have been busy meeting almost every week in the last three months since the TSC was officially chartered. Each sub team started off by understanding and agreeing on deficient areas that they need to address.

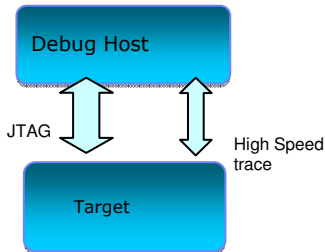
The Application Programming Interface (API) team realizes the incompatible APIs and the individual communicating protocols (P1, P2, P3...etc.) between various debug hosts and the targets in existing implementations. This leads to interoperability and scalability difficulties.



To address these issues the API team’s vision is to create a single Target Communication Framework (TCF) and to define a single set of communication services that can be used by various tool vendors and targets.



The Physical and Logical Connection (PHY) team sees that as core/processor speed becomes higher and higher there is a need of a high speed interface to access trace data from the target for debug. After several rounds of discussion the team concluded that rather than creating a new interface just for Power Architecture it is more appropriate to adopt an existing standard which would reduce both development and product costs. As a result the team is now studying the applicability of the IEEE Nexus 5001™ standard.



While the API and PHY teams address interfaces and protocols, the TGT team defines capabilities in the target to allow the system under test be observed with minimum (or no) intrusion on its operation. These capabilities will be grouped in 1) Core related features, 2) System level features, and 3) Trace features. They will be classified within two levels. Level 1 feature is a required feature. It must be implemented in a Power based product for it to be compliance. Level 2 feature is optional. If included in a Power based product it must be implemented as described in the specification.

During the next several months I anticipate that we will be releasing draft recommendations for members to review. I look forward to your suggestions to help set standards for Power Architecture debug environments.

Additional summary TSC status is provided below.

Sincerely,

Chris Ng
Chairman, Common Debug Interface TSC

Objective: Identify and standardize aspects of common debug environment, interface and methodology (both software and hardware) for Power Architecture

Chair: Chris Ng (IBM) [debug-chair@power.org]

Members: AMCC, Freescale, IBM, Lauterbach, Mentor Graphics, Virtutech, Wind River

Meetings: TSC meets every other Thursday, 12-1PM EST

Home page: <http://www.power.org/apps/org/workgroup/debug/>

Join group: <http://www.power.org/apps/org/workgroup/debug/join.php>

Group Status:

Physical team

- Evaluating IEEE Nexus 5001™ standard
- Defining connector(s), pinouts, cable length

Target team

- Defining core related feature
- Defining system level feature
- Defining trace feature

API team

- Defined Target Communication Framework
- In the process of defining services
- Approaching Multi-core Association for join spec development

Platform Architecture TSC

The Platform Architecture TSC remains active on two main fronts: developing the Embedded Power Architecture Platform Requirements (ePAPR) specification, and recruitment.

First sections of the Embedded PAPR are coming to life, and are beginning to be reviewed, while other sections continue to be developed. Freescale continues as the main contributor. Also, Matt Tyrlik from IBM and John Trail from Freescale have joined as active contributors.

Recruitment continues and is mostly focused on software developers and software companies, as software developers and companies are one of the main customers of ePAPR. Wind River has named John True to work with the subcommittee. Now that MontaVista has joined Power.org, the subcommittee is seeking their involvement. Effort continues to enlist Linux kernel developers, either from member companies, or as developer members via the Developer CALLUP program.

Sincerely,

Dave Willoughby
Chairman, Bus Architecture TSC

Objective: Define and publish base platform arch standards to facilitate development of compliant components and products

Chair: Dave Willoughby (IBM) [parch-chair@power.org]

Members: AMCC, Cadence, Ericsson, Freescale, HCL America, IBM, IPextreme, PA Semi, Thales, Wind River, Wistron

Meetings: Embedded PAPR development bi-weekly conference calls, every other Wednesday 11:30-12:30PM EST. Meetings to discuss server PAPR are scheduled as needed.

Home page: <http://www.power.org/apps/org/workgroup/parch/>

Join group: <http://www.power.org/apps/org/workgroup/parch/join.php>

Specifications: PAPR Version 2.0 [<http://www.power.org/members/developers/specs/PAPR>]

Group Status:

- Scope of embedded PAPR version 1.0 defined. Initial outline of ePAPR specification completed. Developing various boot architecture topics, such as device tree characteristics, with Freescale providing technical leadership.

Key Deliverables:

- 3Q07 - Embedded PAPR draft version 1.0 approved by TSC
- 4Q07 - Embedded PAPR approved and published

Key Next Steps:

- Continue developing ePAPR specification topics

Reference Platform Design TSC

Objective: Produce Reference designs that implement HW/FW Standards for various classes of Power Architecture Platforms to lower overall cost of products and offerings for members of Power.org and PowerPC Ecosystem.

Scope: Reference designs that incorporate various PPC licensees' micros and will become example implementation of classes of PAPR compliant platforms such as Servers, Workstations, Clients, Laptops, High End Embedded, HPC.

Chair: Kaveh Massoudian (IBM) [hvarch-chair@power.org]

Members: Cadence, Freescale, IBM, Mercury Computer, Silicon Application Corporation, Terra Soft, Thales, Wistron

Meetings: Meets bi-weekly with the Platform Architecture TSC, every other Wednesday 11-12 EST.

Home page: <http://www.power.org/apps/org/workgroup/hvarch/>

Join group: <http://www.power.org/apps/org/workgroup/hvarch/join.php>

Group Status:

- Released the Open System Stack in support of the 970MP reference design. Linux and Xen are available from their respective open community source trees. SLOF changes were released into Power.org.
- Working with Power.org partners to produce limited number of platforms for the Linux community to use as software development toolkits.
- Shifting our focus to the embedded space.

Key Deliverables:

- Board schematics
- Board support package made of system firmware and software based on open source initiatives SLOF, Xen, Linux.

Key Next Steps:

- Re-evaluating whether we proceed with the refresh of the I/O subsystem for the 970MP reference design to feature PCI-e Gen2.
- Work with Freescale, AMCC, and P.A. Semi to make available their reference designs.
- Evaluating other proposals from member companies.

System on Chip Design Hierarchy TSC

Objective: Adopt and/or create specifications and standards to enable creation of a world-class SoC design eco-system (tools, methodology, and design enablers) which positions the Power Architecture at the industry forefront and offers designers the easiest path to a successful microprocessor based System-on-a-Chip design.

Chair: Nagu Dhanwada (IBM) interim chair [soc-chair@power.org]

Members: Cadence, Chartered, Ericsson, Freescale, HCL Technologies, IBM, IPextreme, Mentor Graphics, Synopsys

Meetings: As needed

Home page: <http://www.power.org/apps/org/workgroup/soc/>

Join group: <http://www.power.org/apps/org/workgroup/soc/join.php>

Group Status:

- Prepared a SoC methodology gap analysis report targeting areas of highest priority including verification, ESL, tradeoff analysis tools, and models.
- Surveyed Power-based SoC design teams to collect their input on what would lower the barriers to adoption of Power cores in SoCs and improve the efficiency of their SoC development around Power Architecture cores.
- Investigated the SPIRIT IP-XACT standard
- Conducted a preliminary investigation of the issues around the availability of models including functional, cycle-accurate, cycle-approximate models, performance/power models. From an architect exploration and implementation point of view as well as from the application software developer point of view. What is needed, what are the barriers, can power.org agree on common formats.
- Released Power Evaluation Kits (V1.0,V1.5, V2.0) for early analysis of Power/CoreConnect based SoCs
- Prepared recommendation for future directions
- The formation of a new working group to focus on definition and enhancement of system level modeling frameworks for multi-core POWER based SoCs with the following scope is being explored:
 - Improve the availability of models including functional, cycle-accurate, cycle-approximate models, and performance/power models
 - Define modeling frameworks to support architecture exploration of multi-core designs at the system level (ESL), as well as provide a virtual platform for early embedded software development.
 - Leverage current Power Evaluation Kits (current version PEK v2.0) that was released through SoC TSC in Power.org and IBM developerWorks.
 - Define and implement a virtual platform for consumer media and embedded reference systems

Key Next Steps:

- Complete the definition of the first set of topics for the modeling and tools TSC.
 - Proposal from VaST Systems was reviewed by the TSC in this context; next steps are to also hear from other members like Virtutech on the topic of virtual platforms for Power based architectures.

Recommendations:

- Endorse SPIRIT IP-XACT to facilitate Power-based SoC creation
- Ensure availability of all Power busses protocol specification in IP-XACT
- Avoid developing/promoting Power-specific tool/methodology solutions. Instead, leverage existing solutions and industry-wide efforts.
- Explore the establishment of a new working group that will focus on models and simulation

- Accelerate the efforts of the Bus Architecture TSC – key enabler for IP development and SoC design.
- Continue the efforts in the Common Debug Interface TSC
- Conclude the activities of the SoC Design Hierarchy TSC

Application Binary Interface TWG

Objective: Create an unencumbered and up to date 32-bit PowerPC ELF Application Binary Interface Supplement. This will enable independent development of compilers, linkers, and run-timer libraries that interoperate

Chair: Kate Stewart (Freescale), Steven Munroe (IBM) [powerabi-chair@power.org]

Members: IBM, Freescale, CodeSourcery

Meetings: Conference calls every other Friday 12:00-12:45 PM EST

Home page: <http://www.power.org/apps/org/workgroup/powerabi>

Join group: <http://www.power.org/apps/org/workgroup/powerabi/join.php>

Group Status:

- Agreed to use the 64-bit PowerPC ELF ABI Supplement from Free Standards Group (Freestandards.org) as the base for the 32-bit Supplement.
- Obtained permission from the Free Standards Group (now merged into the Linux Foundation <http://www.linux-foundation.org/en/About>), to use the 64-bit ABI source text as starting material and to host the final (new) 32-bit ABI document.
- Agreed to design a single combined source text to generate two documents: 32-bit PowerPC (Linux) ELF ABI Supplement, and 32-bit PowerPC Embedded ELF ABI Supplement.
- Developed taxonomy and tagging system to support the above. This is complicated by the many processor variants (with/without (Binary) floating Point, VMX/Altivec vs SPE, Decimal Floating Point, etc.) within the PowerPC ISA family. These variations impact the ABI for parameter passing, etc.
- Started work on required changes and formatting internal drafts.

Key Deliverables:

- An unencumbered and up to date 32-bit PowerPC ELF ABI Supplement to the System V Application Binary Interface document. Taxonomy that unifies the existing standards
- Scripts that permit generation of ABI according to viewpoints
- 32 bit ABI documented according to taxonomy
- 64 bit ABI documented according to taxonomy
- First public draft 4Q2007
- First release end of 2007

Issues and Dependencies:

- Obtain appropriate copyright assignments etc. to contribute this work to the Linux Foundation.

Disruptive Play TWG

Disruptive Play has expanded its scope to include members from both the Technical and Marketing Committees reflective of its charter to develop Disruptive Play concepts across all of Power.org. We are already seeing Disruptive Play working across other marketing and technical groups to vet ideas and concepts.

Key outputs of the group so far in Q3 are Tein Atkerson’s Membership Networking initiative which allows members to register their interest areas on Power.org website to help identify those companies with common interests that can band together to advance the Power Architecture. One of the first applications of this will be a “birds of a feather” session to be held at the 1st Power Architecture Developer Conference where representatives from companies with common interests can meet in a format similar to “speed dating” to quickly assess whether there is a match.

Disruptive Play is also active with Michael Sullivan’s efforts to develop a solutions database where users will be able to search for products and services available for Power Architecture. A summary of the latest DP topics under discussion by the group:

DP Topic	Sponsor	Status	Description
Sketchbox	Kai Staats	Continuing	Personal computing tablet device
Member Networking	Tein Atkerson	Continuing	“Speed dating” for Power members
Multicore Debug	Warren Savage	Abandoned	Infineon technology repurposed for Power
Solutions Database	Michael Sullivan	Continuing	Database of ecosystem solutions for Power

Sincerely,

Warren Savage
Chair, Disruptive Play TWG

Objective: Provide a collaborative environment in Power.org to develop disruptive plays around Power Architecture.

Chair: Warren Savage (IPextreme) [dp-chair@power.org] and assistant chair Kimberly Fountain (IBM)

Members: Freescale, IBM, IPextreme, Mercury Computer, Rapport, Terra Soft, VaST

Meetings: 1 hour, every other week

Home page: <http://www.power.org/apps/org/workgroup/dp/>

Join group: <http://www.power.org/apps/org/workgroup/dp/join.php>

Group Status:

- Q3 Disruptive Play meetings have started according to the new format described in the June face-face meeting
- Attendance is growing and is now a mixture of marketing and technical people, with a nice cross-pollination of ideas between the two groups
- One existing DP continues from 2006 (Sketchbox) and 3 other DP have been introduced since the start of Q3
- New DP topics for discussion are always needed, and Power.org members are encouraged to join the group to get involved and participate

Key Deliverables:

- Member Networking Survey forms to be added to the Power.org web site by 1 September

Issues and Dependencies:

- Solutions Database requires funding and agreement on implementation plan. Requirements are being gathered to define of scope of work

Key Next Steps:

- Trial Member Networking sessions at the Developer Conference
- Alignment on user interface and implementation plan for Solutions Database

Embedded Hypervisor TWG

Objective: Develop open source hypervisor for embedded PowerPC.

Chair: Hollis Blanchard (IBM) [embedded-hypervisor-chair@power.org]

Members: AMCC, Freescale, IBM, MontaVista, Wind River.

Meetings: No regular schedule; roughly bi-monthly.

Home page: <http://www.power.org/apps/org/workgroup/embedhpv>

Join group: <http://www.power.org/apps/org/workgroup/embedhpv/join.php>

Group Status:

- Developing technical design for hypervisor implementation.
- Collecting requirements and priorities for features such as real-time support and paravirtualization.
- Discussed interface standardization with commercial hypervisor vendor.
- Charter approved; developing scope document.

Key Deliverables:

- Hypervisor for Book E processors, based on the Linux KVM project.
- Paravirtual hypervisor interface specification.
- Project management for hypervisor development.
- Recommendations for core virtualization enhancements for PAAC.
- Recommendations for IO virtualization enhancements for system designers.

Issues and Dependencies:

- Formation of a Power.org policy on open source development.
- Mechanism for interacting with the open source development community.

Embedded Software Framework (a.k.a. Home Media Server) TWG

Objective: The objective of this TWG is to enable embedded software architecture and tools to support Power Architecture multi-core and Power + Accelerators with Home Media Server as an initial targeted collaboration vehicle. The architecture is expected to show the scalability of Power-based solutions across multiple segments such as consumer electronics (as a first target), industrial solution, aerospace and defense, medical, printer and MFP and others.

Chair: Nobuhiro Asai (IBM) [hms-chair@power.org]

Members: Freescale, IBM

Meetings: TBD

Home page: <http://www.power.org/apps/org/workgroup/hms/>

Join group: <http://www.power.org/apps/org/workgroup/hms/join.php>

Group Status:

- A draft Home Media Server White Paper was published and released to TC members. This white paper includes a definition of the HMS, market opportunities, draft architecture, key technologies, relevant consortiums and future direction.
- The focus and objectives were presented at Power.org Communication Day in Japan. The talk was well-accepted with positive feedback from many member/non-member companies.
- Initially the focus is on the infrastructure portion of the layered software stack, and "Hypervisor based Management" was identified as a key differentiator to best utilize Power Architecture.

Key Deliverables:

- Common componentized software framework architecture for various implementations of Power Architecture and some key software components to drive creation of ecosystem.
- A concept chart of hypervisor based management followed by high-level description of it.

Issues and Dependencies:

- Additional members are required to cover the wide-range of consumer electronic devices and develop de-facto architecture and core components.
- Discussion with non-member companies (like network operators and content owners)

Key Next Steps:

- Complete the high-level description of hypervisor based management, and scope/charter document.
- Interlock with the Embedded Hypervisor TWG for hypervisor requirements and with the ePAPR team for potential enhancements to the device tree.

Software Initiatives (SWI) TWG

As you can see above we've added two new TWGs for proposed TSCs: The Embedded Hypervisor TWG and the Application Binary Interface TWG (please see above for more details).

In addition, we are having regular calls on Tuesdays (please visit the SWI TWG site on Power.org for more information) to discuss general software topics/possible new software initiatives.

We also just kicked off a new sub-team SWI-[EDT] that will take a look at early development tools (aka pre-silicon development tools) to see what's available for Power in this area and how Power stacks up against some of the competitors. For more information please visit the SWI homepage.

Additional status summary information can be found below:

Sincerely,

Nina Wilner
Chairman, Software Initiatives TWG

Objective: Help build a well rounded applications portfolio for Power Architecture.

Chair: Nina Wilner (IBM), [swi-chair@power.org]

Members: IBM, Freescale, Terra Soft Solutions, Virtutech, VaST

Meetings: Tuesdays and Fridays, 11:00 AM EST

Home page: <http://www.power.org/apps/org/workgroup/swi/>

Join group: <http://www.power.org/apps/org/workgroup/swi/join.php> (or email Nina)

Group Status:

- Discussing and evaluating new possible software initiatives for power
- Discussing linkage/procedures between power.org and open source projects.

Key Deliverables:

- Startup [EDT] subteam
- Process for open source projects linked to power.org

Random Bytes

Forgot your Power.org username and/or password?

Go to the link below and enter the email address you used to enroll in Power.org:
http://www.power.org/kmembership_info/request_password/. A link to create a new password and/or username will be emailed to you.

Unsubscribe from Power.org general email list

To unsubscribe from the members email list and not receive any general announcements, update your Power.org account at http://www.power.org/kmembers/person/change_personal_info and set the "Receive Members Email" option to "No". **NOTE:** You will continue to receive emails from any committees you have joined.

Acronyms

ABI	Application Binary Interface
BoD	Board of Directors
cPAPR	Consumer PAPR
ePAPR	Embedded PAPR
ISA	Instruction set architecture
PAAC	Power Architecture Advisory Council
PAPR	Power Architecture Platform Requirements
SoC	System on Chip
TC	Technical Committee
TSC	Technical Subcommittee – A formal workgroup chartered by the Board of Directors to create specifications and implementations
TWG	Technical Workgroup – An informal workgroup created to explore the formation of a TSC
VIC	Venture capitalist innovation council