

Technical Committee Newsletter

4Q2007

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2007 Year in Review

Power.org will begin its third year of enabling collaborative innovation in January of 2008, so I would like to take this opportunity to reflect on this year's accomplishments and later in the Technical Committee update section, I'll comment on the directions for 2008.

Let me first extend my appreciation to the many member contributors for your support, commitment and most of all, your passion and energy for making this Power Architecture collaborative model successful. We still have much to improve as any new model does, but 2007 can be logged in the books as an impressive year in terms of collaborative team accomplishments. Each of us know the many challenges we all face daily with limited resources, short timelines and the like – seems like that's a perennial challenge, but in spite of these challenges many of you have contributed and executed in Power.org very well. On behalf of the Power.org Board of Directors and the Committee Chairs, I would like to say thank you for a great year and that we look forward to your continued enthusiasm and dedication in 2008. So now, let's look and recap what an impressive scorecard we had in 2007!

Focus and **Collaboration Assets** were the operative words for us in 2007. We worked hard this year to narrow and refocus our technical initiatives based on the market analysis and member feedback from 2006. We placed emphasis on embedded, consumer, SoC and software, based on your direct input. We also commissioned collaborative primary market research to study our Power Architecture market, our collective competition and to search out and focus on new opportunity areas for Power Architecture so we all could benefit from growing our business on Power. We studied over five dozen sub-segments with the leading market research and analysis firm, International Data Corporation (IDC) and will deliver the findings this quarter exclusively to our members. One quick take-away from that research is that Power Architecture remains a driving architecture in the industry over the next five years and we have several segments of “#1” share to boast to our customers and analysts! It's up to all of us to expand the use of Power Architecture designs in the new growth areas. Corporate members can read the report to find out where. Special thanks go to [Michael Sullivan \(IBM\)](#), [Fawzi Behmann \(Freescale\)](#), and [Tein Atkerson \(Power.org\)](#) for their project management and necessary ‘cat-herding’ of this collaborative asset.

To further demonstrate our collaboration efforts, and with a tremendous sponsorship from many of you, we demonstrated to the embedded systems industry just how much of a force we are -- regardless of who's custom motorcycle was sitting in a booth next to ours! At this year's Embedded Systems Conference in the spring, we were front-and-center at the exhibit doors and provided a strong presence on the floor while creating visibility and awareness for our members.

From attention getting AMCC aisle-banners hanging from the ceiling, to every single attendee wearing a badge-holder, we created strong Power-brand visibility. With over a dozen individual and joint-company pedestals, we let our demonstrations and booth staffs tell the attendees how Power.org was leading the way on industry collaboration around Power Architecture technology.

The awareness of Power.org was further promoted by our sponsoring an evening *Power Night at the Museum*. Introducing best-selling authors, Chip and Dan Heath, as they shared their "sticky" insights found in their new book, "Made to Stick - Why Some Ideas Survive and Others Die" and featured a night of noshing and networking with other innovators and industry leaders. It was viewed as such a great success that many of you voiced the need to continue that type of event in 2008. Kudos go to the leadership provided by [Debby Hindus \(Rapport\)](#) and [Pierre Golde \(Denali Software\)](#) who orchestrated and delivered this very successful ESC Power.org booth and evening event.

During the summer, Freescale, VaST Systems, Rapport, CSIP and IBM co-hosted the **Power.org Communication Day – Asia** "road show". Local member teams from Freescale, VaST Systems, Rapport, Wind River, XGI, Silicon Application Corp, Sony, Tundra, Xilinx, AMCC, CSIP and IBM participated, contributed and represented Power.org as we visited four countries in two weeks. We communicated, educated and shared our collaborative Power Architecture product and technology information to our China, Taiwan, Japan and Korea audiences including members, sales teams and customers. We also learned about geographic specific requirements to improve Power Architecture activity internationally. As a result of positive feedback, we plan to continue that regional focus in 2008 and you will be hearing more of that very soon from Fawzi Behmann, our new Marketing Committee Chair. A gracious thank you to all the co-hosts, especially [VaST Systems, Freescale, and IBM](#) for providing their own resources above and beyond the Power.org funding to help make this a success. Additionally, a thank you goes to [XGI](#) for hosting a dinner meeting.

In a true collaborative effort between the Technical and Marketing Committees, Power.org was able to deliver new industry-leading collaborative tools and assets ranging from **ISA v2.05 Specification, SoC Gap Analysis, Mid- and Low-performance Bus Report** updates, **PLB4 Interoperability Specification, 970 Platform Reference Design** and availability of **a high performance Linux Developers Toolkit**. The latter being the result of over one year of collaboration among member companies in Power.org such as IBM, Broadcom, Wistron, Terra Soft Solutions and XGI. This platform is available as a toolkit to developers and its design is available to all members who wish to make their own products. Great job to all the Technical Subcommittees and Marketing Committee members who helped produce and deliver those assets.

Last, but certainly not least, we delivered two firsts in 2007: an initial **Power Architecture Solutions Framework** and a **Power Architecture Developer Conference (PADC)**! Never before in our industry, has any one organization, delivered a multi-supplier, open, collaborative architecture solution catalog and an education and networking event like Power.org did this past September. The successful attendance of close to 400 developers and managers at the Power Architecture Developer Conference in Austin, Texas proved that our ecosystem is eager for access to solution and technology information. It was confirmed by the media as well as by the ten industry analysts who attended the pre-conference Analyst Dinner, that Power.org -- all of you-- did a fantastic job of delivering value at the event. As one analyst was quoted, "... for a first year effort, this one was an A+. I would definitely attend again. Very impressive all the way around."

It's now up to us to continue to enable that ecosystem to use and adopt our Architecture and technology. I will share with you that this is recognized by the Power.org planning teams and they will respond to that ecosystem demand in 2008. Connect to the Marketing and Technical Committees to hear more about that. Thanks go to the many contributors who made PADC a success, especially [Jesse Stein](#), [Pat Johnson](#), [Kaveh Massoudian](#), [Lovdy Hamm](#), [Michael](#)

[Sullivan, Joan Woolery, Tein Atkerson and Corridor Communications](#) for their un-ending desire and passion to 'get it done right'!

Summarizing, in 2007, we demonstrated to the industry, and to ourselves, through a variety of proof-points that we can collaborate to innovate in our ecosystem and it can produce real business and technological benefits. We collectively developed, built and promoted specifications, reports, tools, research, created awareness, visibility and new business opportunities and relationships from networking for all of us. We have ramped up a community-driven marketing and branding 'engine' that we plan to continue leveraging throughout 2008. We developed initial Power Architecture Solutions website content that will be enhanced in 2008 to become a true solutions database and "Portal." We will continue to focus on areas our members have asked for such as awareness, visibility, networking opportunities, and enhancing and expanding our academic initiatives with universities.

We have great momentum going into 2008. With your continued support we'll make 2008 an even better year.

Sincerely,

Michael Paczan
Chairman, Power.org Technical Committee
tech-chair@power.org

Announcements

- **Power.org hosted the first-ever Power Architecture™ Developer Conference 24-25 September, Austin Convention Center, Austin, Texas**

What difference collaboration makes! We successfully held this first ever Developer Conference dedicated to Power Architecture on 24-25 September, at the Austin Convention Center. The best practices of all the member companies combined with the leadership of our Platinum Sponsors (AMCC, Freescale, IBM and Power.org) resulted in an inaugural conference that some attendants rated as one of the best technical conferences they had ever attended.

Austin, Texas is the spiritual home of Power Architecture where Freescale, IBM and AMCC have their main architect and development teams for Power Architecture. This made the event very special as we were able to make available many of the thought leaders and experts of Power Architecture. Over 70 hours of technical curriculum, labs and panels provided a valuable experience with tangible collateral for the attendees and member companies.

All sessions and presentations were recorded and are available to Power.org members at: http://www.power.org/devcon/07/Session_Downloads/

Mike Paczan, Power.org Technical Committee Chair, kicked off the event's theme of breaking down the barriers to innovation by breaking a symbolic barrier on stage. He also helped introduce three excellent and energetic keynotes from the Platinum sponsors, AMCC, Freescale, and IBM.

It was really exciting to see some of our key customers present some of their future research areas related to Power Architecture. Many Power.org member companies presented their latest offerings and architecture innovations with enough technical depth to spark lively discussions and exchanges on ideas on common issues faced by our members. In addition, many vendors displayed their tools and offerings for Power Architecture-based hardware and software development in the "Landscape" which also served as our reception area for the first day where we had Power Architecture prize giveaways for the lucky people in attendance.

Overall feedback was very positive and the conference planning committee has gathered and consolidated all the feedback to incorporate into enhancements for the next developer conference. Thanks to the conference planning committee and the technical content review committee who made this event world class and meaningful.

- **Online Power Architecture Solutions Catalog**

Phase 1 of an online Power Architecture solutions catalog was launched in September as the Power Architecture Solutions Framework [www.power.org/solutions_stack]. Many of you sent feedback via the online comment form and now the Marketing and Technical Committees have joined forces to build Phase 2. It goes by several names (solutions catalog, solutions database, solutions portal), but whatever the name, the goal is to educate and motivate developers to select Power Architecture technology over the competition by guiding them to specific solution options and suppliers of products and services that can best help them accomplish their development objectives.

Phase 2, slated for 2Q2008, will feature robust search/browse capabilities, detail company and product information, plus identification of compatible products and services.

- **New Members**

Welcome new member [E2V](#) to the Power.org family.

Technical Updates

Technical Committee

Our major TC meeting focus has been on two core items: 1) PADC preparation and 2) 2008 Strategy and Plans. Additional details are provided below.

Sincerely,

Michael Paczan
Chairman, Power.org Technical Committee

Objective: Establish and maintain the overall technical vision and goals for Power.org. Responsible for forming and supervising Technical Subcommittees (TSC) that develop reports, specifications and reference designs.

Chairman: Michael Paczan (IBM) [tech-chair@power.org]

Members: AMCC, Cadence, Denali, Ericsson AB, Freescale, IBM, Mentor Graphics, P.A. Semi, Rapport, Silicon Application, Sony, Synopsys, Thales, VaST Systems, Venture Corp, Virtutech, Wind River, Wistron, Xilinx

Meetings: Monthly conference calls. Quarterly face-to-face meetings.

Home page: <http://www.power.org/apps/org/workgroup/tech/>

Join group: <http://www.power.org/apps/org/workgroup/tech/join.php>

Group Status:

- The Technical Committee and BOD approved the formation of two new technical subcommittees in October. These are:
 - Power ABI – Kate Stewart, Chair (Freescale)
 - Embedded Hypervisor – Hollis Blanchard, Chair (IBM)Details on these TSCs can be obtained by contacting the Chairs directly.
- Power.org collaboration goals and objectives 2008 were reviewed and finalized at our November face to face meetings. The high level summary is shown in Table 1. Our primary Technical Subcommittee focus areas for 2008 will be:
 - Common Debug Interface (CDI)
 - ePAPR
 - Power ABI
 - Embedded Hypervisor
 - Modeling / Virtual Platforms
 - Power Solutions Portal contributions
- The following Technical Subcommittees have completed their work scope and will end-of-life in Dec '07: 1) Bus Architecture 2) Ref Platform 3) SoC Design Hierarchy. The CDI and Modeling / Virtual Platforms TSCs supplant the SoC TSC. Any follow-up reference platform TSC is dependent on a member company stepping up with a leadership proposal. Should that occur, then a new TSC formation process would begin.

TABLE 1: 2008 Power.org Goals, Objectives, and Measurements

GOAL	Strategic Business Objectives	2008 Power.org Tactical Objectives Summary	2008 Power.org Contribution	Impact	Key Measurements
<p>Support increasing the competitive value of the Power Architecture in the market place and its architectural share</p>	<ul style="list-style-type: none"> Strengthen and promote the global Power Architecture ecosystem Contribute to lowering development expenses Support growing Power Architecture Market Adoption 	<ul style="list-style-type: none"> Increase member tangible value 	<ul style="list-style-type: none"> Demonstrate increase in business linked to Power.org initiatives Unified reference resource (public catalog of Power Architecture offerings/solutions) Technology standards 	<p>Influence awareness and pref for Power Arch solutions with Developers</p>	<p>Ecosystem Product Coverage Member Satisfaction Solutions Stack Database usage</p>
		<ul style="list-style-type: none"> Lower the barriers to adoption of Power Architecture in embedded and consumer systems 	<ul style="list-style-type: none"> 1st Release of ePAPR Spec: Jan 08, 2nd Release of ePAPR: 2H08 Release Open Source Embedded Hypervisor: TBD Update Power ABI Enhance Operating System and open source driver support for Power: On-going 	<p>Makes it easier for Developers to create products with Power Arch Technology Increased business opportunity</p>	<p>Release of ePAPR Hypervisor spec and related open source code Power ABI</p>
		<ul style="list-style-type: none"> Lower the barriers to adoption of and cost of development with Power cores in SoCs 	<ul style="list-style-type: none"> Develop modeling improvements with improved ESL tool integration and support Release Common Debug Interface (CDI) Spec: 1H08 	<p>Lower cost and simplified development of processor and boards</p>	<p>Operating Modeling/Virtual Platform TSC</p>
		<ul style="list-style-type: none"> Increase Power Architecture demand through research, awareness and education 	<ul style="list-style-type: none"> Architecture positioning, branding and messaging Market research Member and customer events Community training and education Influencer relations – Press, Analysts and Universities Community and industry communication 	<p>Increased awareness Increased skills</p>	<p>Event Feedback Market Research Report(s)</p>
		<ul style="list-style-type: none"> Continue convergence ISA and updates to meet new req'ts 	<ul style="list-style-type: none"> Release ISA v2.06: 4Q08 (embedded and server enhancements) 	<p>Sustain Power ISA competitiveness in the markets it serves</p>	<p>Release of ISA v2.06 Member Satisfaction</p>
		<ul style="list-style-type: none"> Enhance connection to Developer and Academic Community 	<ul style="list-style-type: none"> Regional Events/Summits, Webcasts Enhance Power.org Website content to attract developers and facilitate networking Contribute to regional academic and marketing events 	<p>Increased awareness and skill among Dev community and students about Power Arch Tech</p>	<p>Events/Webinar participation and surveys Student participation in "Contests"</p>
		<ul style="list-style-type: none"> Create a sustainable Power.org operating model 	<ul style="list-style-type: none"> Operate to a balanced budget: membership dues relative to expenses Explore increasing sponsorship funding model Manage recruitment and retention - Retention Target: 80% 	<p>Support basic viability of Power.org as a community resource</p>	<p>Member feedback Balanced budget Shared investment across members</p>

Power Architecture Advisory Council

Objective: Discuss ISA contributions to the Power Architecture ISA and vote on whether to make recommendations to IBM regarding such ISA contributions.

Chair: Wolfram Sauer (IBM) [paac-chair@power.org]

Members: Freescale, IBM

Home page: <http://www.power.org/apps/org/workgroup/paac/>

Specifications:

- **Power ISA Version 2.05** (.pdf 8MB) [to be published soon]
- **Power ISA Version 2.04** (.pdf 7MB)
[\[http://www.power.org/resources/downloads/PowerISA_204-FINAL.Public.pdf\]](http://www.power.org/resources/downloads/PowerISA_204-FINAL.Public.pdf)
- **Power ISA Version 2.03** (.pdf 7MB)
[\[http://www.power.org/resources/downloads/PowerISA_203.Public.pdf\]](http://www.power.org/resources/downloads/PowerISA_203.Public.pdf)

Group Status:

- Power ISA Version 2.05 was approved by the PAAC and has been presented to the Power.org Technical Committee. A summary of changes was presented at the 14 November TC meeting. Power ISA Version 2.05 will be publicly available in December.

Key Deliverables:

- Dec 07 - Power ISA Version 2.05.
- 4Q08 - Power ISA Version 2.06.

Application Binary Interface TSC

Objective: Create an unencumbered and up to date 32-bit PowerPC ELF Application Binary Interface Supplement. This will enable independent development of compilers, linkers, and run-timer libraries that interoperate

Chair: Kate Stewart (Freescale), Steven Munroe (IBM) [powerabi-chair@power.org]

Members: IBM, Freescale, CodeSourcery

Meetings: Conference calls every other Friday 12:00-12:45 PM EST

Home page: <http://www.power.org/apps/org/workgroup/powerabi>

Join group: <http://www.power.org/apps/org/workgroup/powerabi/join.php>

Group Status:

- Developed taxonomy and tagging system. This was complicated by the many processor variants (with/without (Binary) floating Point, VMX/Altivec™ vs. SPE, Decimal Floating Point, etc.) within the PowerPC ISA family. These variations impact the ABI for parameter passing, etc.
- Created first internal draft according to Taxonomy; reviewed all chapters with team.
- Reworking areas determined to have too much similarity with SysV ABI wording to avoid copyright issues.
- Need to add newly evolved precedents from Linux to 32 bit draft.

Key Deliverables:

- An unencumbered and up to date 32-bit PowerPC ELF ABI Supplement to the System V Application Binary Interface document. Taxonomy that unifies the existing standards
- Scripts that permit generation of ABI according to viewpoints
- 32 bit ABI documented according to taxonomy
- 64 bit ABI documented according to taxonomy
- First public draft 1Q2008 (changed due to additional work from review for copyright issues.)
- First release 32 bit ABI 2Q2008
- First release 64 bit ABI 4Q2008

Issues and Dependencies:

- Obtain appropriate copyright assignments etc. to contribute this work to the Linux Foundation.

Bus Architecture TSC

The Bus Architecture TSC moved the latest release of the PLB4 Interoperability Specification (PLB4 IOS v1.1) into a public, searchable location within the Power.org web site. Links to both the PLB4 Architecture Specification and the PLB4 IOS may be found at the following link, <http://www.power.org/resources/downloads/>. By making the PLB4 IOS easily accessible in a searchable location, the hope is that developers of new PLB4 cores will adhere to the guidelines and ensure compatibility with existing PLB4 cores.

The Bus Architecture TSC is in the process of writing the Embedded Bus Architecture Report. The purpose of the report is to formally recommend and explain the selection of both the CoreConnect and AMBA bus families as the recommended low and mid-performance buses.

To date, no member company has offered it's version of a high-performance bus to the Bus Architecture TSC. The belief within some member companies is that each proprietary high-performance bus offers a unique competitive advantage that would be lost if a single high-performance bus was selected and used by all the member companies. However, the position held by the Bus Architecture TSC is that each company will incur much more cost developing their own IP for CPUs, accelerators, memory controllers, and bridges to other buses. They will also need to develop their own verification IP, models and monitors. Some of these efforts will yield a real competitive advantage, but much will be a redundant effort, where the only significant difference is in the bus interface itself.

The Bus Architecture TSC work will conclude with the release of the Embedded Bus Architecture Report. I would like to thank each of the members for contributing their time, energy, and valued opinions. It's been a pleasure to serve on this committee, knowing that its findings and recommendations have influenced and will continue to influence design decisions made on SoCs based on Power Architecture. I would especially like to recognize the efforts and contributions made by the previous chair, Rich Nicholas of IBM, as well as Kathy Werner of Freescale, and Marc Greenberg of Denali.

Sincerely,

Jason Hopp
Chairman, Bus Architecture TSC

Objective: Define a hierarchy of bus architectures and support structures to standardize the bus interconnect in Power based SoCs, enabling rapid reuse, lower development costs, and increased compatibility.

Chair: Jason Hopp (IBM) [barch-chair@power.org]

Members: AMCC, Cadence, Denali, Ericsson, Freescale, HCL Technologies, IBM, Mercury Computer, P.A. Semi, Synopsys

Meetings: Thursdays 12:00-1:00 PM EST

Home page: <http://www.power.org/apps/org/workgroup/barch/>

Join group: <http://www.power.org/apps/org/workgroup/barch/join.php>

Specifications:

- **PLB4 Interoperability Specification:**
http://www.power.org/resources/downloads/resources/downloads/PLB4_Interop_Spec.pdf

Group Status: In the process of generating the Embedded Bus Architecture Report

Key Deliverables:

- | | |
|---------------------------------------|----------|
| • Vision and direction white paper | Complete |
| • Mid-performance bus report | Complete |
| • PLB4 Interoperability Specification | Complete |
| • Low-performance bus report | Complete |
| • Bus Architecture Deep Dive | Complete |

- Updated PLB4 Interoperability Specification available Complete
- Embedded Bus Architecture Report Dec
- End-of-life Bus Architecture TSC 31 Dec 2007

Common Debug Interface TSC

The Application Programming Interface (API) team published a white paper on a Common Debugging Framework last month. It detailed the lack of uniform debug interfaces, environments and methodologies in current Power Architecture™ implementations and proposed a solution to these problems. Below is an abstract of the white paper:

“The API workgroup has looked at existing debugging standards and concluded that something more scalable, flexible, and powerful is needed. The purpose of this paper is to document the vision for resolving the lack of a unified and scalable communication mechanism between the target and the host for the purpose of debug, performance analysis and other development activities. It gives a high-level view of the problem, the proposed communication framework, and examples of communication services.”

Download the white paper at <http://www.power.org/resources/downloads/>.

The Physical and Logical Connection (PHY) team is about to finish the first draft specification for Physical Connection for High-Speed Serial Trace. On the electrical side, a High Speed Serial Trace Port Protocol based on Aurora Interface is being specified. For the connector, careful considerations were given on the requirements needed to support bit rate up to 6.25 GB/s. To provide flexibility, three connector options are defined. A 28-pin version supports up to 2 channels. The 46-pin version supports up to 4 channels while the 70-pin version provides a full 8-channel support. The team is finalizing the pin outs.

The Target (TGT) team is also close to having its first draft specification for Target Debug Capabilities ready for comment soon. The team is finishing up the last couple of sections. The specification is focused on Core (non Trace), System (non Trace), and Trace related features.

Stay tuned for the release of draft versions of the specification from the PHY team and the TGT team for member comments. I look forward to hearing your suggestions.

Additional summary TSC status is provided below.

Sincerely,

Chris Ng
Chairman, Common Debug Interface TSC

Objective: Identify and standardize aspects of common debug environment, interface and methodology (both software and hardware) for Power Architecture

Chair: Chris Ng (IBM) [debug-chair@power.org]

Members: AMCC, Freescale, IBM, Lauterbach, Mentor Graphics, Virtutech, Wind River

Meetings: TSC meets every other Thursday, 12-1PM EST

Home page: <http://www.power.org/apps/org/workgroup/debug/>

Join group: <http://www.power.org/apps/org/workgroup/debug/join.php>

Group Status:

Physical team

- First draft Physical Connection for High-Speed Trace spec 4Q07
- Physical Connection for High-Speed Trace spec 1Q08

Target team

- First draft Target Debug Capabilities spec 4Q07
- Target Debug Capabilities spec ` 1Q08

API team

- Vision and Strategy white paper Complete
- First draft API/TCF spec 1Q08
- API/TCP spec 2Q08

Embedded Hypervisor TSC

Objective: Develop open source hypervisor for embedded PowerPC.

Chair: Hollis Blanchard (IBM) [embedded-hypervisor-chair@power.org]

Members: AMCC, Freescale, IBM, LynuxWorks, MontaVista, Wind River.

Meetings: No regular schedule; roughly bi-monthly.

Home page: <http://www.power.org/apps/org/workgroup/embedhpv>

Join group: <http://www.power.org/apps/org/workgroup/embedhpv/join.php>

Group Status:

- Working group approved to become a Technical Subcommittee.
- Discussing hypercall interface standardization with multiple hypervisor implementors.
- Defining a hypercall ABI standard.

Key Deliverables:

- Hypervisor for Book E processors, based on the Linux KVM project.
- Paravirtual hypervisor interface specification.
- Project management for hypervisor development.
- Recommendations for core virtualization enhancements for PAAC.
- Recommendations for IO virtualization enhancements for system designers.

Issues and Dependencies:

- Formation of a Power.org policy on open source development.
- Mechanism for interacting with the open source development community.

Platform Architecture TSC

The Platform Architecture TSC remains active on two main fronts: developing the Embedded Power Architecture Platform Requirements (ePAPR) specification, and future initiatives.

The final sections of the Embedded PAPR are nearing completion and final reviews are not far away. Freescale and IBM are the main contributors, with Stuart Yoder, John Trail, (Freescale); Matt Tyrlik and David Gibson (IBM) busy completing various sections. Thanks to our main contributors as well as the active involvement on the mailing list from many participants helping hammer out the details of this evolving specification.

As embedded PAPR version 1.0 nears completion, the TSC is considering initiatives for a follow-on version next year, with thoughts of adding run time abstractions and virtualization extensions.

Also, with the completion of version 1.0 nearing, the TSC is working on activities to help gain adoption of the specification, including reference platforms and reference firmware.

Increased participation is always welcome. If you'd like to contribute technically or also help deciding on how best to evangelize these standards in the industry or your company's activities, please join the TSC!!

Sincerely,

Dave Willoughby
Chairman, Platform Architecture TSC

Objective: Define and publish base platform arch standards to facilitate development of compliant components and products

Chair: Dave Willoughby (IBM) [parch-chair@power.org]

Members: AMCC, Cadence, Ericsson, Freescale, HCL America, IBM, IPextreme, PA Semi, Thales, Wind River, Wistron

Meetings: Embedded PAPR development bi-weekly conference calls, every other Wednesday 11:30-12:30PM EST. Meetings to discuss server PAPR are scheduled as needed.

Home page: <http://www.power.org/apps/org/workgroup/parch/>

Join group: <http://www.power.org/apps/org/workgroup/parch/join.php>

Specifications:

- PAPR Specification V2.2 (Workstation, Server):
<http://www.power.org/members/developers/specs/PAPR>

Group Status:

- Embedded PAPR version 1.0 in final reviews

Key Deliverables:

- Dec 07 - Embedded PAPR draft version 1.0 approved by TSC
- Feb 08 - Embedded PAPR approved and published

Key Next Steps:

- Complete review of ePAPR specification version 1.0

Reference Platform Design TSC

Objective: Produce Reference designs that implement HW/FW Standards for various classes of Power Architecture Platforms to lower overall cost of products and offerings for members of Power.org and PowerPC Ecosystem.

Scope: Reference designs that incorporate various PPC licensees' micros and will become example implementation of classes of PAPR compliant platforms such as Servers, Workstations, Clients, Laptops, High End Embedded, HPC.

Chair: Kaveh Massoudian (IBM) [hvarch-chair@power.org]

Members: Cadence, Freescale, IBM, Mercury Computer, Silicon Application Corporation, Terra Soft, Thales, Wistron

Meetings: Meets bi-weekly with the Platform Architecture TSC, every other Wednesday 11-12 EST.

Home page: <http://www.power.org/apps/org/workgroup/hvarch/>

Join group: <http://www.power.org/apps/org/workgroup/hvarch/join.php>

Group Status:

- Released the Open System Stack in support of the 970MP reference design. Linux and Xen are available from their respective open community source trees. SLOF changes were released into Power.org.
- Announced the availability of the 970MP LINUX Developers TOOLKIT at the Power Architecture Developers Conference.

Key Deliverables:

- Board schematics
- Board support package made of system firmware and software based on open source initiatives SLOF, Xen, Linux.

Key Next Steps:

- Working with Power.org partners to produce limited number of platforms for the Linux community to use as software development toolkits.
- Shifting our focus to the embedded space and use of Virtual Platforms.
- We will sunset this TSC at the end of 2007.

System on Chip Design Hierarchy TSC

Objective: Adopt and/or create specifications and standards to enable creation of a world-class SoC design eco-system (tools, methodology, and design enablers) which positions the Power Architecture at the industry forefront and offers designers the easiest path to a successful microprocessor based System-on-a-Chip design.

Chair: Nagu Dhanwada (IBM) interim chair [soc-chair@power.org]

Members: Cadence, Chartered, Ericsson, Freescale, HCL Technologies, IBM, IPextreme, Mentor Graphics, Synopsys

Meetings: As needed

Home page: <http://www.power.org/apps/org/workgroup/soc/>

Join group: <http://www.power.org/apps/org/workgroup/soc/join.php>

Group Status:

- Prepared a SoC methodology gap analysis report targeting areas of highest priority including verification, ESL, tradeoff analysis tools, and models.
- Surveyed Power-based SoC design teams to collect their input on what would lower the barriers to adoption of Power cores in SoCs and improve the efficiency of their SoC development around Power Architecture cores.
- Investigated the SPIRIT IP-XACT standard
- Conducted a preliminary investigation of the issues around the availability of models including functional, cycle-accurate, cycle-approximate models, performance/power models. From an architect exploration and implementation point of view as well as from the application software developer point of view. What is needed, what are the barriers, can power.org agree on common formats.
- Released Power Evaluation Kits (V1.0,V1.5, V2.0) for early analysis of Power/CoreConnect based SoCs
- Prepared recommendation for future directions
- The formation of a new working group to focus on definition and enhancement of system level modeling frameworks for multi-core POWER based SoCs with the following scope is being explored:
 - Improve the availability of models including functional, cycle-accurate, cycle-approximate models, and performance/power models
 - Define modeling frameworks to support architecture exploration of multi-core designs at the system level (ESL), as well as provide a virtual platform for early embedded software development.
 - Leverage current Power Evaluation Kits (current version PEK v2.0) that was released through SoC TSC in Power.org and IBM developerWorks.
 - Define and implement a virtual platform for consumer media and embedded reference systems

Key Next Steps:

- Complete the definition of the first set of topics for the modeling and tools TSC.
 - Proposal from VaST Systems was reviewed by the TSC in this context; next steps are to also hear from other members like Virtutech on the topic of virtual platforms for Power based architectures.
 - A virtual reference platform TSC proposal from VaST was reviewed. Due to commonality with the scope of the proposed modeling and tools TSC, work is on-going to come up with a charter proposal that merges the virtual reference platform TSC and the modeling and tools TSC.

Recommendations:

- Endorse SPIRIT IP-XACT to facilitate Power-based SoC creation
- Ensure availability of all Power busses protocol specification in IP-XACT

- Avoid developing/promoting Power-specific tool/methodology solutions. Instead, leverage existing solutions and industry-wide efforts.
- Explore the establishment of a new working group that will focus on models and virtual platforms
- Accelerate the efforts of the Bus Architecture TSC – key enabler for IP development and SoC design.
- Continue the efforts in the Common Debug Interface TSC.
- Conclude the activities of the SoC Design Hierarchy TSC at the end of 2007.

Disruptive Play TWG

Disruptive Play has expanded its scope to include members from both the Technical and Marketing Committees reflective of its charter to develop Disruptive Play concepts across all of Power.org. We are already seeing Disruptive Play working across other marketing and technical groups to vet ideas and concepts.

In Q3 and to date in Q4 we have executed on several important ideas for Power.org, primarily driven by the compelling event of the first Power Architecture Developer Conference. The Member Networking initiative was kicked off by extending the member profile information capabilities of the Power.org web site to allow people to indicate areas of interest. We invited people to update their profiles and provide us with areas of interest and from this we organized introductions between members with like interests at a “Birds of a Feather” session at the conference. The DP team is now considering how this should be taken forward. In addition, we were able to implement the first phase of the Solutions Database (aka Solutions Stack) on the Power.org web site with is simply a static listing of available Power Architecture solutions. This initiative is now being taken to the next level by a tiger team led by Joan Woolery to develop a database oriented approach with more advanced capabilities. A key output of the team in Q4 will be refining the requirements for Phase 2 and planning its implementation within available budget.

The DP TWG is actively asking for more contribution to the working group with innovative, disruptive ideas in either marketing or technical areas.

A summary of the latest DP topics under discussion by the group:

DP Topic	Sponsor	Status	Description
Sketchbox	Kai Staats	Continuing	Personal computing tablet device
Member Networking	Tein Atkerson	Graduated	“Speed dating” for Power members
Multicore Debug	Warren Savage	Abandoned	Infineon technology repurposed for Power
Solutions Database	Joan Woolery	Continuing	Database of ecosystem solutions for Power
SoC IP Repository	Warren Savage	New	Discuss what role Power.org should play

Sincerely,

Warren Savage
Chair, Disruptive Play TWG

Objective: Provide a collaborative environment in Power.org to develop disruptive plays around Power Architecture.

Chair: Warren Savage (IPextreme) [dp-chair@power.org] and assistant chair Kimberly Fountain (IBM)

Members: Freescale, IBM, IPextreme, Mercury Computer, Rapport, Terra Soft, VaST

Meetings: 1 hour, every other week

Home page: <http://www.power.org/apps/org/workgroup/dp/>

Join group: <http://www.power.org/apps/org/workgroup/dp/join.php>

Group Status:

- Member networking initiative resulted in a richer member profile sheet that can be used to help identify members with similar interests.
- Solutions Database project resulted in the first phase of the project being enabled on the Power.org web site, with planning for the second phase in progress. See http://www.power.org/solutions_stack

Key Deliverables:

- Planning and requirements for the Solutions Database project to be completed in the Q4 timeframe according to the available budget.

Key Next Steps:

- Tiger team on Solutions Database to align on high level requirements and present to the board for approval.

Software Initiatives (SWI) TWG

The scope proposals of two TSCs (Application Binary Interface TSC and Embedded Hypervisor TSC) were approved by the board. These two groups have now commenced their technical work as formal TSCs. (Please refer to respective sections in this news letter).

We added a new sup-group to the work of this SWI TWG. This new subgroup is looking specifically at early- or pre-silicon development tools for Power Architecture. This new sub-group, SWI-EDT, meets regularly on Tuesdays at 2PM CST. This group is developing an inventory of available early development tools for Power Architecture and is documenting this in a spreadsheet. This work will be followed by a gap analysis.

In parallel we are discussing and evaluating the need for an EDT framework and specifications which would allow tools to work together smoothly and would create a “plug-n-play” like environment of EDT tools.

In addition, we had regular calls on Tuesdays (please visit the SWI TWG site on Power.org for more information) to discuss general software topics/possible new software initiatives. Because of low participation we temporarily discontinued this separate generic call and rolled the more generic discussion into the EDT call. We are however considering some new discussions (i.e. multi-core, multiprocessor software environments, open source projects and open shadow organization, etc.)

Additional status summary information can be found below:

Sincerely,

Nina Wilner
Chairman, Software Initiatives TWG

Objective: Help build a well rounded software ecosystem and application portfolio for Power Architecture.

Chair: Nina Wilner (IBM), [swi-chair@power.org]

Members: IBM, Freescale, Terra Soft Solutions, Virtutech, VaST

Meetings: Tuesdays 3:00 PM EST

Home page: <http://www.power.org/apps/org/workgroup/swi/>

Join group: <http://www.power.org/apps/org/workgroup/swi/join.php> (or email Nina)

Group Status:

- Discussing and evaluating new possible software initiatives for Power Architecture
- Discussing linkage/procedures between Power.org and open source projects.
- Creating requirements document for open shadow organization and Power.org management of open source projects
- Creating EDT inventory

Key Deliverables:

- Startup EDT sub-group
- EDT inventory spreadsheet
- Gap analysis
- EDT framework or new TSC to develop specifications for EDT framework
- Process for open source projects linked to Power.org

Random Bytes

Forgot your Power.org username and/or password?

Go to the link below and enter the email address you used to enroll in Power.org:
http://www.power.org/kmembership_info/request_password/. A link to create a new password and/or username will be emailed to you.

Unsubscribe from Power.org general email list

To unsubscribe from the members email list and not receive any general announcements, update your Power.org account at http://www.power.org/kmembers/person/change_personal_info and set the "Receive Members Email" option to "No". **NOTE:** You will continue to receive emails from any committees you have joined.

Acronyms

ABI	Application Binary Interface
BoD	Board of Directors
ePAPR	Embedded PAPR
ISA	Instruction set architecture
PAAC	Power Architecture Advisory Council
PAPR	Power Architecture Platform Requirements
SoC	System on Chip
TC	Technical Committee
TSC	Technical Subcommittee – A formal workgroup chartered by the Board of Directors to create specifications and implementations
TWG	Technical Workgroup – An informal workgroup created to explore the formation of a TSC
VIC	Venture capitalist innovation council